PERFORMANCE EVALUATION OF MULTILEVEL INVERTER BASED ON TOTAL HARMONIC DISTORTION (THD)

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Abstract

In general Pulse width modulation (PWM) techniques of a voltage source inverter (VSI) need a sinusoidal reference signal and triangular carrier signal to generate the required modulating signals for the desired output. Modifications in modulating techniques can be considered in two ways, namely modified reference and modified carrier. The existing multilevel carrier based pulse width modulation (PWM) strategies have no special provisions to offer good quality output, besides lower order harmonics are introduced in the spectrum, especially at low switching frequencies. In this paper a pulse width modulation (PWM) scheme for multilevel inverters is proposed. The proposed PWM scheme generates the inverter leg switching times using only the sampled amplitudes of reference phase voltages. The proposed PWM technique does not involve any sector identification and considerably reduces the computation time when compared to the conventional space vector PWM technique. The proposed PWM signal generation scheme can be used for any multilevel inverter configuration. The main objective of this work is the most relevant control and modulation methods by a new reference/carrier based PWM scheme for a Diode clamped and Cascaded multilevel inverters are proposed for 5-level inverters. The performance indexes used in this comparison is total harmonic distortion (THD).

Index Terms— *multilevel inverter, total harmonic distortion.*

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1. INTRODUCTION

Multilevel power conversion technology is a very rapidly growing area of power electronics with good potential for further development. The most attractive application of this technology is in the medium-to-high-voltage range, motor drives, power distribution, and power conditioning applications. In recent years, industry demands power in the megawatt level. Controlled ac drives in the megawatt range are usually connected to medium-voltage network. Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels.In general multilevel inverter can be viewed as voltage synthesizers, in which the high output voltage is synthesized from many discrete smaller voltage levels.

The main advantages of this approach are summarized as follows:

- They can generate output voltages with extremely low distortion and lower (dv/dt).
- They can operate with a lower switching frequency.
- Their efficiency is high (>98%) because of the minimum switching frequency.
- They are suitable for medium to high power applications.

The selection of the best multilevel topology for each application is often not clear and is subject to various engineering tradeoffs. By narrowing this study to the DC/AC multilevel power conversion technologies that do not require power generation. Multilevel inversion is a power conversion strategy in which the output voltage is obtained in steps thus bringing the output closer to a sine wave and reduces the total harmonic distortion (THD). Various circuit configurations namely diode clamped, flying capacitor and cascaded, etc., have been proposed.

1.1 System Configuration

Inverter Configuration	Diode-Clamp	Flying-Capacitors	Cascaded-inverters
Main switching devices	2(m-1)	2(m-1)	2(m-1)
Main diodes	2(m-1)	2(m-1)	2(m-1)
Clamping diodes	(m-1) (m-2)	0	0
DC bus capacitors	(m-1)	(m-1)	(m-1)/2
Balancing capacitors	0	(m-1) (m-2)/2	0

Table.1. Comparison of Switches

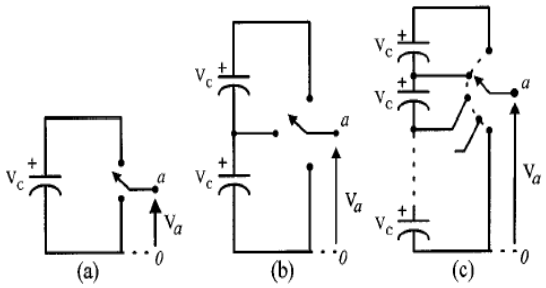


Fig. 1 Multilevel concept for (a) two level (b) three level and (c) n- level

Multilevel inverter structures have been developed to overcome shortcomings in solid-state switching device ratings so they can be applied to higher voltage systems. The multilevel voltage source inverters unique structure allows them to reach high voltages with low harmonics without the use of transformers. The general function of the multilevel inverter is to synthesize a desired ac voltage from several levels of dc voltages as shown. The table shows that the number of main switches and main diodes needed by the inverters to achieve the same number of voltage levels is the same. Compares the power component requirements per phase leg among the three multilevel voltage source inverter mentioned above. Clamping diodes do not need in flying-capacitor and cascaded-inverter configuration, while balancing capacitors do not need in diode clamp and cascaded-inverter configuration. Implicitly, the multilevel converter using cascaded-inverters requires the least number of components.

2. INVERTER TOPOLOGIES

2.1 Diode Clamped Multilevel Inverter

The most commonly used multilevel topology is the diode clamped inverter, in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. In general the voltage across each capacitor for an N level diode clamped inverter at steady state is *Vdc/n-1* .Although each active switching device is only required to block *Vdc/n-1*, the clamping devices have different ratings. The diode-clamped inverter provides multiple voltage levels through connection of the phases to a series of capacitors. According to the original invention, the concept can be extended to any number of levels by increasing the number of capacitors. In general for an N level diode clamped inverter, for each leg 2 (N-1) switching devices, (N-1) * (N-2) clamping diodes and (N-1) dc link capacitors are required. When N is sufficiently high, the number of diodes and the number of switching devices will increase and make the system impracticable to implement. If the inverter runs under pulse width modulation (PWM), the diode reverse recovery of these clamping diodes becomes the major design challenge.

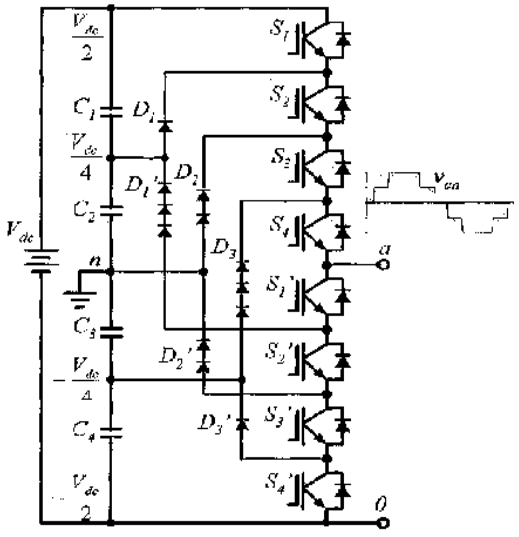


Fig.2. Single leg five level DCMLI

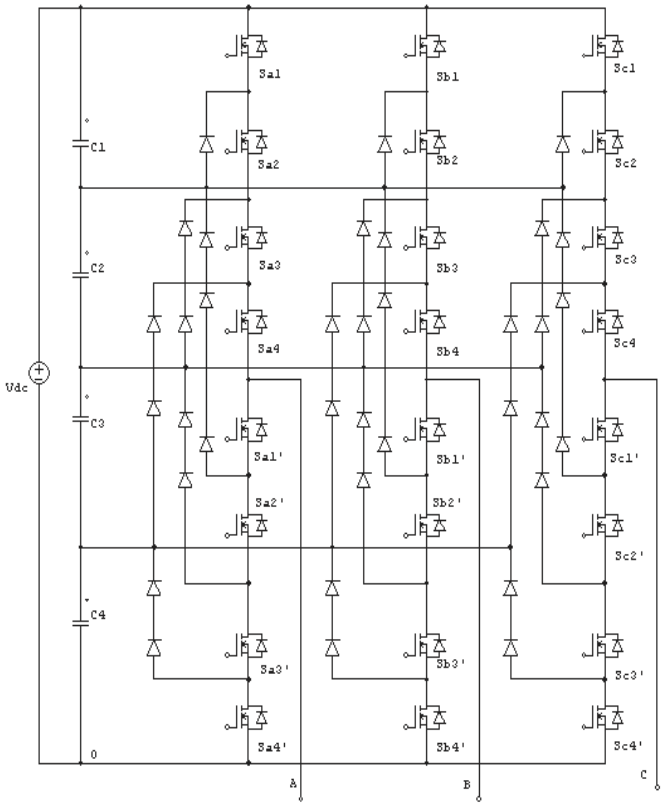


Fig.3. Three Phase 5-Level Diode Clamped Inverter

Output Voltage	Switching sequence							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a1}^1	S_{a2}^1	S_{a3}^1	S_{a4}^1
+VDC/2	1	1	1	1	0	0	0	0
+VDC/4	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
-VDC/2	0	0	0	1	1	1	1	0
-VDC/4	0	0	0	0	1	1	1	1

Table.2. Switching Sequence of Single Leg DCMLI For 5-Level

2.2. Cascaded Multilevel Inverter

One of the early applications of the series connection of single-phase full-bridge inverter topology was for plasma stabilization in 1988. This modular approach has since been extended to include three-phase systems as well.Arguably, the overall complications and cost of the isolated sources for each full bridge is overall not too serious drawback and is offset by the advantages of modular construction. The modularity of this structure allows easier maintenance and provides a very convenient way to add redundancy into the system. The cascade H-bridge inverter is a cascade of H-bridges, or H-bridges in a series configuration. A single phase 5-level cascade H-bridge inverter is shown in fig (2) and the three phase cascade H-bridge inverter for five-level inverter is shown in fig (3). A N level Cascaded H bridge inverter consists of series connected (N-1)/2 number of cells in each phase. Each cell consists of single phase H bridge inverter with separate dc source. There are four active devices in each cell and can produce three levels 0, $V_{dc}/2$ and $-V_{dc}/2$. Higher voltage levels can be obtained by connecting these cell in cascade and the phase voltage van is the sum of voltages of individual cells, $v_{an}= v_1 + v_2+ v_3 + :::: + v_n$. For a three phase system, the output of these cascaded inverters can be connected either in configuration

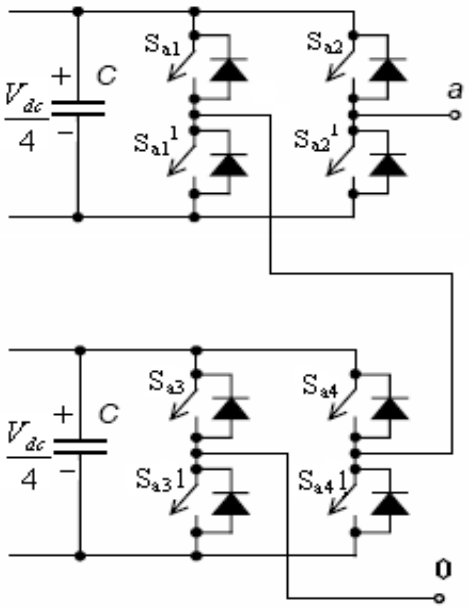


Fig.4. Single Leg Five Level Cascaded Inverter

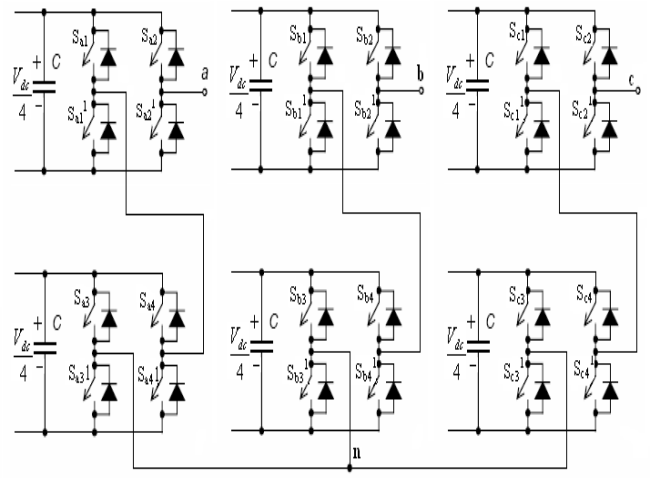
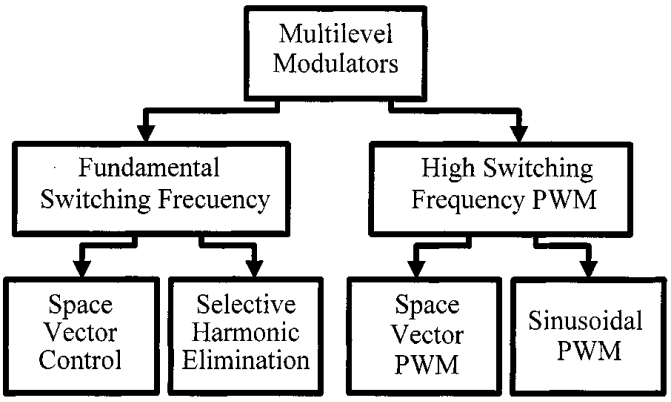


Fig.4. Three Phase Five level Cascaded Multilevel Inverter

Output Voltage	Switching sequence							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a1}^1	S_{a2}^1	S_{a3}^1	S_{a4}^1
0	1	1	0	0	0	0	1	1
Vdc	1	0	0	0	0	1	1	1
2Vdc	1	0	1	0	0	1	0	1
-Vdc	0	1	1	1	1	0	0	0
-2Vdc	0	1	0	1	1	0	1	0

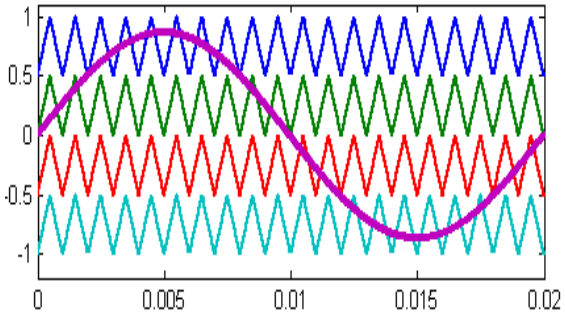
Table.3.Switching Sequence of Single Leg DCMLI For 5-Level

3. MODULATING STATEGIES OF MULTILEVEL INVERTERS



3.1 Sinusoidal Pulse Width Modulation Technique

Modulation techniques for voltage source inverters may be carrier based or carrier-less and open loop or closed loop. These modulation or control techniques for multilevel voltage source inverters are classified. Simulation investigation of different multilevel control techniques have been presented in this paper. The SPWM technique is considered for study in this paper. It is the simple technique to be implemented. In the SPWM technique, a triangular carrier wave at a high witching frequency is compared with the sinusoidal reference wave at a fundamental output frequency. The control principle of the SPWM is to use several triangular carrier signals keeping only one modulating sinusoidal signal. Two and four triangular carrier signals are needed for three- and five-level inverters, respectively. The carriers have the same frequency fc and the same peak-to-peak amplitude Ac. The zero reference is placed in the middle of the carrier set. The modulating signal is a sinusoid of frequency fm and amplitude Am. At every instant, each carrier is compared with the modulating signal. Each, comparison switches the switch 'on' if the modulating Signal is greater than the triangular carrier assigned to that switch.

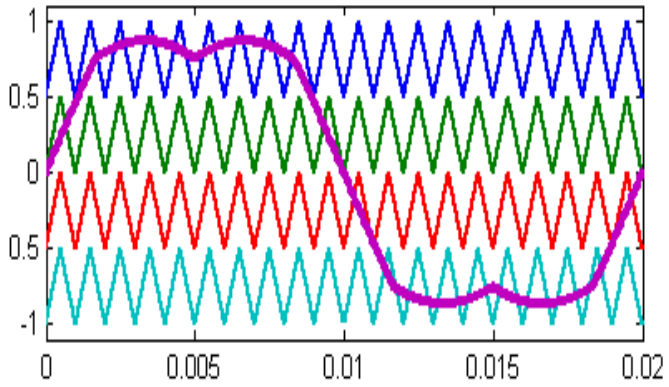


3.2 Modified Space Vector PWM

In the SPWM scheme for two-level inverters, each reference phase voltage is compared with the triangular carrier and the individual pole voltages are generated, independent of each other [6]. To obtain the maximum possible peak amplitude of the fun common mode voltage, Voffset1, is added to the reference phase voltages [9, 1], where the magnitude of Voffset1 is given by

$$V_{offset1} = \frac{-(V_{max} + V_{min})}{2} \text{ --(1)}$$

In (1), Vmax is the maximum magnitude of the three sampled reference phase voltages, while Vmin is the minimum magnitude of the three sampled reference phase voltages, in a sampling interval. The addition of the commons mode voltage, Voffset1, results in the active inverter switching vectors being centered in a sampling interval, making the SPWM technique equivalent to the modified reference PWM technique.



4. SIMULATION RESULTS FOR DIODE CLAMPED INVERTER

4.1. Using Sinusoidal PWM:

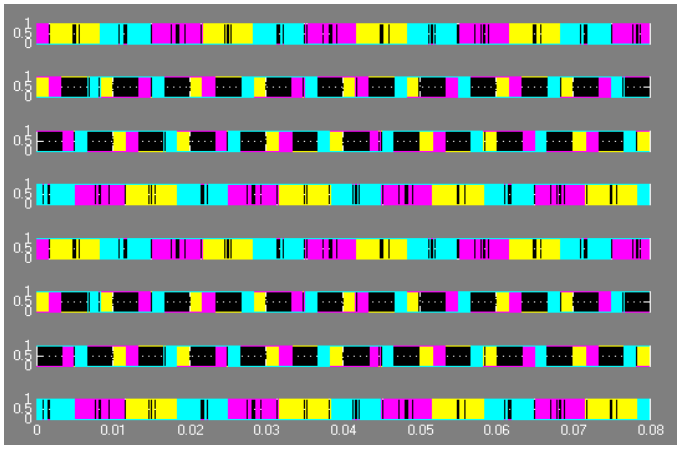


Fig.5. Waveforms of pulses

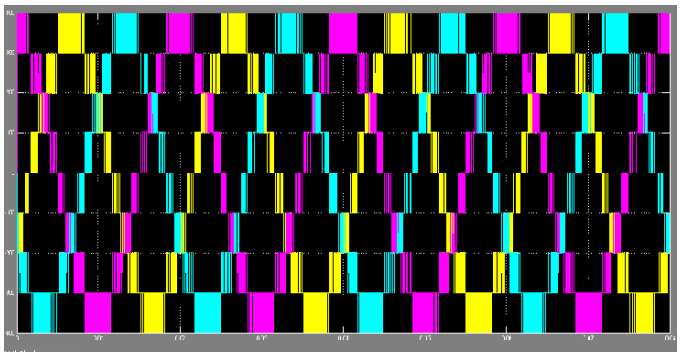


Fig.6. Output voltage

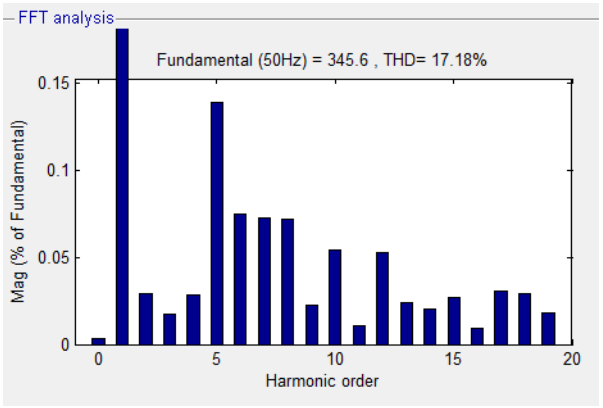


Fig.7. Harmonic spectrum

4.2. Using Modified Space Vector:

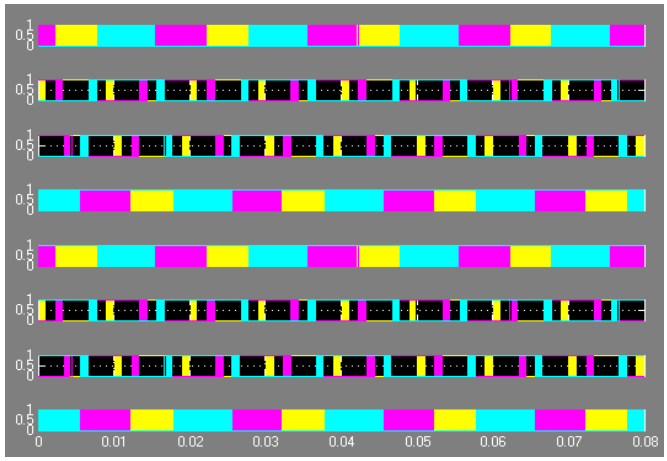


Fig.8. Waveforms of pulses

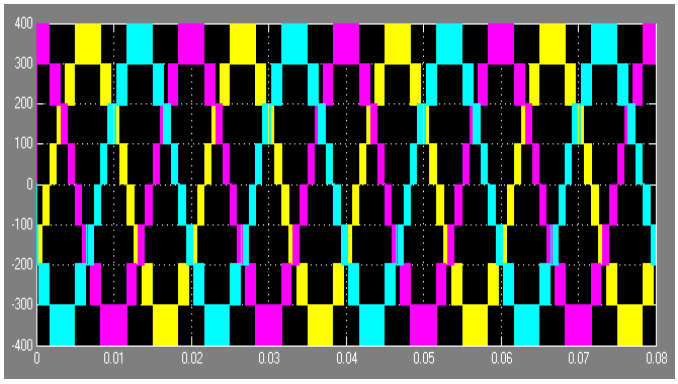


Fig.9. Output voltage

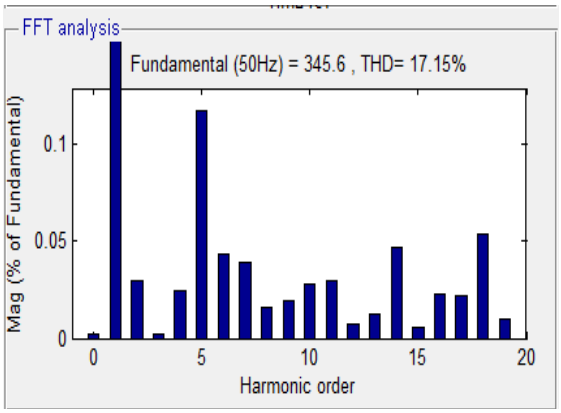


Fig.10. Harmonic spectrum

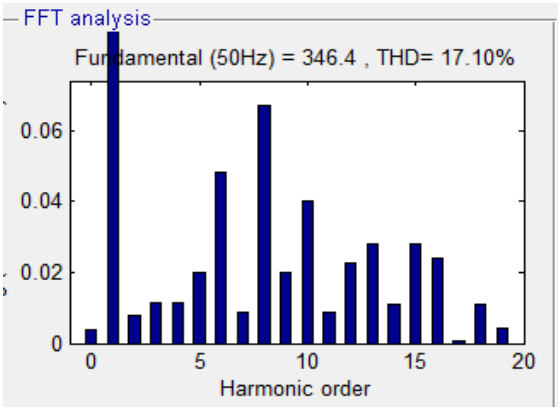


Fig.13. Harmonic spectrum

5. SIMULATON RESULTS FOR CASCADED MULTILEVEL INVERTER

5.1. Using Sinusoidal PWM

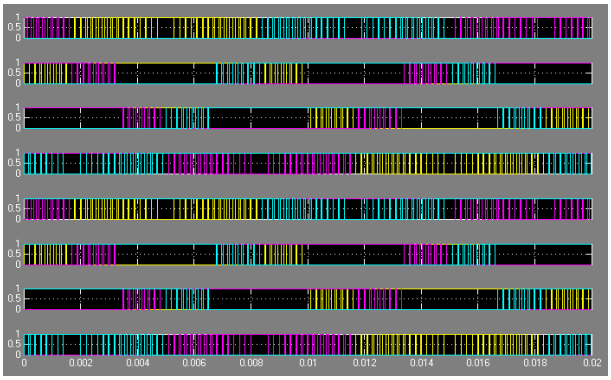


Fig.11. Waveforms of pulses

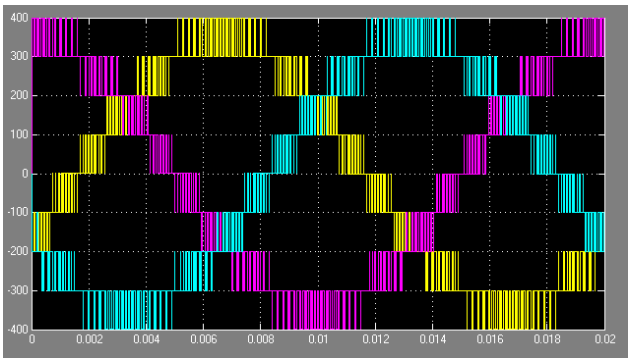


Fig.12. Output voltage

5.2. Using Modified Space Vector

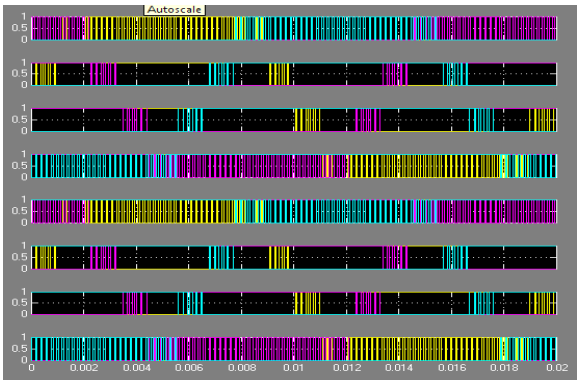


Fig.14. Waveforms of pulses

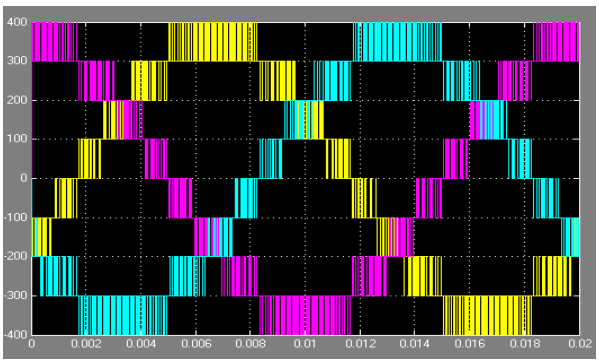


Fig.15. Output voltage

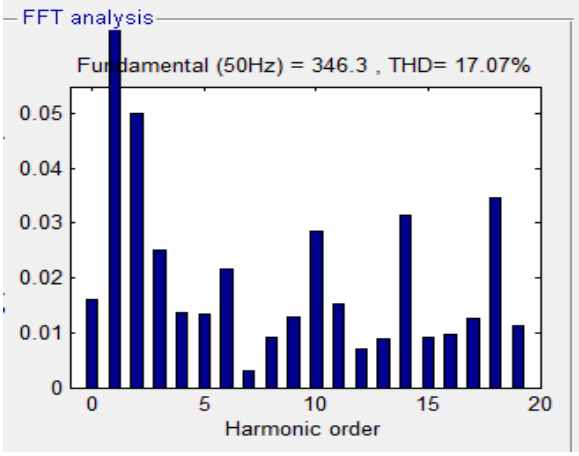


Fig.16. Harmonic spectrum

6. CONCLUSION

The diode clamped and Cascaded 3-phase five level multilevel inverter is simulated for sinusoidal PWM technique and modified space vector PWM technique. The simulation results with harmonic spectrum are presented in this paper. it is concluded that modified reference SVPWM technique has given good harmonic spectrum with fundamental (346.3) and THD (17.07%) when compared with other techniques for Cascaded five level inverter.

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