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ARM PROCESSOR BASED RADAR VELOCITY MEASURING ALGORITHM

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Abstract

The real-time monitoring of vehicles velocity has become essential for traffic safety. Therefore, in order to improve the method of monitoring the velocity of vehicles on road, this paper has designed a new radar velocity-measuring system which is based on ARM processor. This system is based on Doppler principle and spectral estimation algorithm, in its hardware design part, and it takes full use of the underlying resources of ARM processor, to achieve sample, digital signal processing and peripheral control in the separate ARM core. In the software design part, it analyses the main program flow, at the same time, since the ARM processor does not support hardware floating-point operations, it puts forward the usage of fixed-point numbers to store and calculate floating-point numbers, Which makes the data loading and storage minimization And it uses ARM assembly language to write the core algorithm and takes full advantage of the 5-stage pipeline of ARM processor, to achieve the right register allocation and instruction scheduling for fine-grained control, and also to avoid the pipeline inter locks. Experimental results indicate that the accuracy of this velocity measurement system can reach ±1km/h. It not only can be used in traffic enforcement agencies, but also has low cost, low power consumption advantages.

Index Terms: *ARM Processor, Radar, Analog to Digital Converter(ADC),FFT Algorithm.*

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1. INTRODUCTION

With the rapid development of the transportation industry, on the one hand, it promotes the economic and social prosperity, on the other hand, the modern intelligent traffic management and the traffic safety has been pushed to an unprecedented height. This extensive research topic has become an important world issue, and how to measure the velocity of vehicles is an important part of it. Speeding has been the main causation for traffic accidents, referred to "the first killer", so the real-time monitoring of vehicles velocity has become essential for traffic management and traffic safety.

At present, there are many ways of velocity measurement, including the coil method (Bruce R.Hellinga, 2002), image processing method (Huei-Yung Lin, Kun-Jhih Li and ChiaHong Chang,2008), laser Doppler velocimetry (LIU Changwen, LUYao,LIU Jie and LU Fei, 2004), radar velocity measuring system etc (W.Kleinhempel, D.Bergmann and W.Stammler,1992). The last two methods have been widely used due to its portability and high accuracy advantages.The laser Doppler velocimetry, though it has high accuracy, long effective distance advantages, but also has short comings, as only in the stationary state to use, easy to be found by driver, expensive and soon. The radar velocity-measuring system, although its effective distance is less than the laser velocimetry, it also can meet the requirements of high accuracy and can be used in stationary and motion state, moreover it has become popular due to the mature technology and affordable price. As early as 1970s, western countries began to use radar velocity-measuring system, but these products are analog, large, and with low accuracy. To 1990s, a new radar velocity-measuring system appeared, which contained integrated circuits digital signal processor, and worked in the Ka-band, compared with the analog one, it has advantages of high accuracy, and small size.

In respect of implementation technology, several generations of radar velocity-measuring system has appeared with the development of microcontrol and microprocessor chip. The first generation product uses single chip to implement. This single chip needs to complete the control functions, also needs to complete the core algorithm of velocity-measuring system, but these algorithms are limited to a few simple, low-

precision algorithms, such as counting cycles method and so on. The final product can achieve velocity measurement, but the accuracy is not enough, and the speed of systems operation is very slow. The second generation product uses single chip plus DSP (Digital Signal Processing) processor, which uses the traditional dual-core mode, that is, one single chip is to deal with the control system and another separate DSP processor is to complete the part of digital signal processing. This way can achieve the core algorithm that contains a large number of complex operations. The accuracy and speed of this generation products are much higher than the first generation products. With the emergence and extensive application of ARM processors, its rich peripheral control module and the underlying hardware resources make it possible to achieve the second generation product, that is to say, just use of ARM single-core will be able to complete the traditional dual-core task, not only can greatly simplify the complex hardware design of the second generation product, but also have low cost, low power consumption advantages (Andrew N.Sloss, Dominic Symes and Chris Wright, 2005). Therefore, the innovation of this paper lies in using ARM processor to achieve the radar velocity-measuring system. It can be used in traffic enforcement agency for measuring speeding violations, and will be a new trend in the development of the radar velocity- measuring system.

2. THE COMPOSITION AND RELATED PRINCIPLES OF RADAR VELOCITY-MEASURING SYSTEM

The ARM-based radar velocity-measuring system mainly includes two parts: radar transceiver front end and radar signal processing system. As millimetre wave radar has advantages of narrow angle, high resolution, anti-interference ability, small size in light of the design of radar transceiver front end, this design uses Doppler millimetre-wave transceiver front end, which is developed by Innocent Company. Its operating frequency is 24 GHz, linear polarization, orthogonal field mixing, the output power is 50 mW, the antenna gain is 25 dB, and it can meet the performance indicators requirement for highway velocity measurement, but also takes into the power consumption. As for the radar signal processing system, the specific design will be highlighted in Chapter III. Firstly it will introduce the basic principles of radar velocity measurement and the signal processing principles in the radar signal processing system.

2.1. DOPPLER PRINCIPLES OF RADAR VELOCITY MEASUREMENT

Measurement of the target velocity by radar mainly uses the Doppler effect to carry out. The fixed-frequency electromagnetic waves which are launched by the radar transceiver front end, will be bounced back when it encounters objects in the transmission process. If the encountered objects are stationary, then the frequency of bounced back waves will not change; If the encountered objects moved toward the direction of wave source, the waves bounced back at this time will be compressed, its frequency will increase; On the contrary, if the movement away from the wave source, the received echo frequency will be lower than the launch frequency. Among them, the increase or decrease of frequency value is called the Doppler frequency, decided by the following equation:

$$f_d = \frac{2v_r}{C} f_0 \qquad (1)$$

In the equation: f_d is Doppler frequency, v_r is the velocity of target vehicle, C is the speed of light, f_0 is the launch frequency of radar wave, here it is equal to 24 GHz. From (1) we can get:

$$v_r = \frac{f_d . C}{2 f_0} \qquad (2)$$

From (2) we can see other variables are known, as long as the Doppler frequency be worked out, we can calculate the target vehicle velocity.

2.2. THE SIGNAL PROCESSING PRINCIPLES OF THE SYSTEM

From the above Doppler principles we can see that through estimating the Doppler frequency of radar echo signal, we can complete the velocity estimation of target vehicle. Among them, the measurement error of frequency directly affects the measurement results of velocity. Period gram method is a kind of classical spectral estimation, it not only has the high accuracy of frequency estimation, but also can complete real-time signal processing. Therefore, we choose his method as the core algorithm of frequency measurement in the system.

Period gram method takes the N points observation data $x_N(n)$ of random signal x(n) as a power limited signal, and directly takes the Fourier transform of $x_N(n)$, then it can get $x_N(e^{jw})$. Count the amplitude square of $x_N(e^{jw})$, which is divided by N, and make it as the estimation of real power spectrum. Use $P_{PER}(k)=1/N(|X_N(K)|^2$ to express the power spectrum which is estimated by Period gram method, then we can get the equation as follows:

$$\hat{P}_{PER}(k) = \frac{1}{N} |X_N(k)|^2 \qquad (3)$$

Since $x_N(K)$ can be calculated by FFT, $P_{PER}(k)$ can be easily calculated too, so the frequency of the signal will be able to be identified through solving the signal's power spectrum.

3. THE DESIGN OF RADAR SIGNAL PROCESSING SYSTEM

Unlike DSP processor, ARM processor is not a dedicated digital signal processing chip, there is no single command to achieve the multiply-accumulate and parallel data access. However, with the ARM architecture fortified, making ARM slowly can be applied to many DSP applications. For ARM9TDMI and the beyond ARM processor, simply by careful clever software design, it can get a higher performance in digital signal processing section of the application system, while in the control part of the application system can also significantly better than DSP chips. Therefore, radar signal processing system based on ARM is entirely feasible, and it has simple hardware design, low cost and low power consumption advantages. Here we choose the S3C2410A Samsung ARM chip to be the main processor of the system.

3.A. THE HARDWARE DESIGN OF RADAR SIGNAL PROCESSING SYSTEM

The system's hardware architecture mainly includes three parts: pre-treatment part of the radar signal, digital signal processing part, and peripherals control part of the system.

3.A.1.THE DESIGN OF RADAR SIGNAL PRETREATMENT PART

Radar transceiver front end will launch 24 GHz frequency electromagnetic waves, which are reflected back by the moving target, and through mixing, the radar transceiver front end will output a 100mv weak sinusoidal signal, the frequency of the signal namely is the Doppler frequency that we want to collect. However, the deferent radar signal has a variety of interference, including the low frequency and high frequency interference, which requires a band-pass filter to prevent the interference signal, pass the useful signal. And this deferent radar signal is very weak too, therefore, this paper designed a adjustable amplifier circuit, so that through the low-frequency amplified, analog signal will be sent to the ADC (Analog to Digital Converter) module of ARM for sampling. Since S3C2410A has a 10-bit ADC with 8-channel analog inputs and its analog input range is 0-3.3V, we need to add a 3 V limiter circuit to ensure that ARM processor does not get burned. The hardware block diagram of this part is shown in Fig. 1.

For the band-pass filter design, we use the general purpose active filter MAX275 of U.S. MAXIM Company to achieve the fourth-order Butterworth active filter for radar signal, and set the transmission bands are 300Hz-16 kHz. So by (2), immediately we can see velocity measurement range is 5-250km/h, which is fully able to meet the traffic law enforcement's velocity measurement requirements; For the adjustable amplifier design, we choose the integrateddualsupplyoperationalAmplifierOP07,firstly use OP07 to constitute a voltage follower, it is mainly used to increase input impedance and decrease Output impedance. Then the output of voltage follower connect another OP07 non-inverting amplifier circuit, it's input resistance is 2kΩ, the feedback resistance is 100kΩ adjustable resistor, so that magnification factor will be in the 0-34dB adjustable scope.

Fig 1: Hardware block diagram of the radar signal pre-treatment part

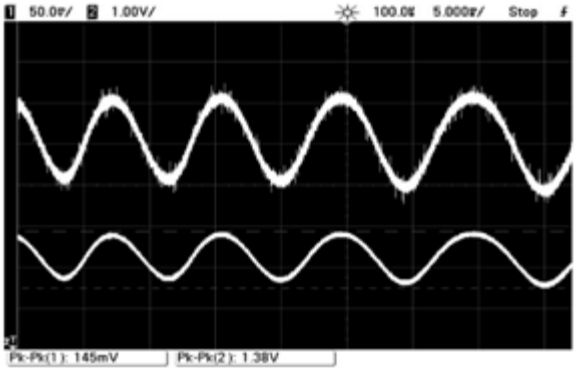

Fig 2: The effect diagram of amplification and filtering

The design of Radar signal pre-treatment part is directly related to the back end software's velocity measurement accuracy, that is, even if the back end frequency estimation algorithm is very accurate, as long as the radar signal's pre-treatment has a little distortion, it also will reduce the back end velocity measurement accuracy. Fig. 2 is the effect diagram of amplification and filtering, at the top of the figure is the original radar signal which with more clutter, but the bottom waveform after amplification and filtering had achieved well filtering and undistorted amplification for the radar signal. The design of the amplification and filtering part

deriving from a large number of experiments test has strong innovative and practicability.

3.A.2. THE DESIGN OF DIGITAL SIGNAL PROCESSING AND PERIPHERALS CONTROL PART

ARM processor is the core of these two parts' hardware design. First, through the radar signal pre-treatment, the analog signal will be put into the ARM's ADC module for sampling, convert into a digital signal, and then use ARM to carry out digital signal processing, ultimately use ARM control module to communicate with the PC, to set the speeding threshold value in the keyboard, to display the real-time velocity, to set speeding violation alarm by a buzzer and some other functions. The hardware block diagram of these two parts is shown in Fig. 3.

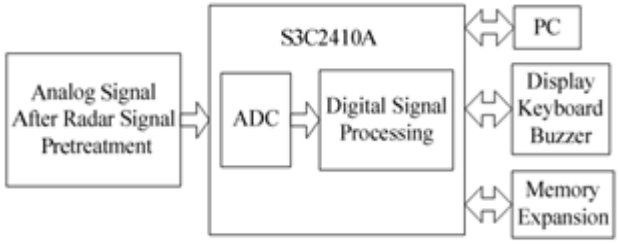

Fig3: Hardware block diagram of these two parts

The digital signal processing part fully use ARM's underlying hardware resources, and is achieved by software design, that is, the digital signal which is produced from the ADC module will use the spectrum analysis to estimate the frequency and velocity. This part will be amply described in the following software design part; The design of the system's peripherals control part, such as LCD circuits, keyboard circuit, buzzer circuit and so on, they all are common circuit, so this paper will no longer describe its composition. In addition, because S3C2410A processor only has a 4kB internal RAM, therefore, usual way is to expand the dynamic RAM, as well as the Nand Flash and Nor Flash outside the S3C2410A. Here it is designed to: expand a 64MB SDRAM, a 64MB Nand Flash and a 2MB Nor Flash. This memory expansion design, not only meets the storage needs of radar system, but also provides storage resources for embedding system to achieve more powerful velocity measurement and additional features.

3.B. THE SOFTWARE DESIGN OF RADAR SIGNAL PROCESSING SYSTEM

The system's software design uses mixed programming which includes ARM assembly language and C programming language, in which the ARM assembly language is to achieve the key algorithm -- FFT algorithm; while pre-treatment part of the radar signal and follow-up processing section of the spectrum analysis use C language for the program.

The main task of radar signal processing system's software design is to carry out sampling, operation pre-treatment, spectrum operation, output and display of the operation results for the Doppler radar signal which passed from the radar transceiver front end. The main flowchart of its software design is shown in Fig. 4.

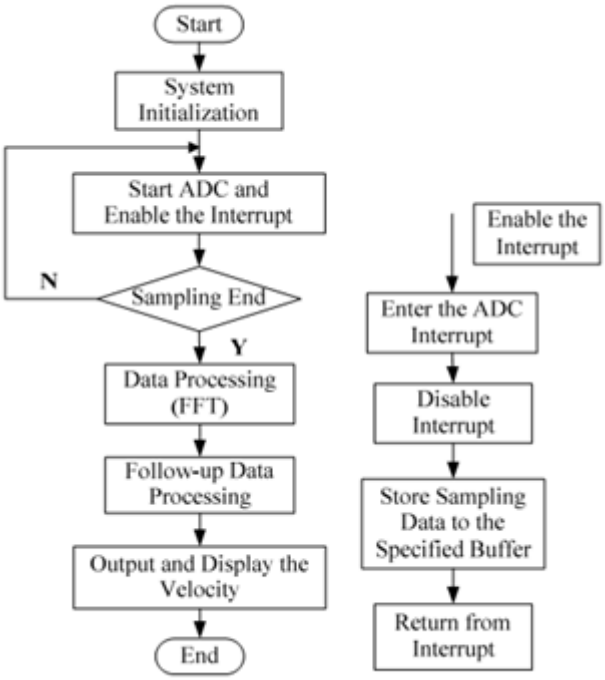

Fig4: Main Flow chart

The software operation of system is divided into two stages, the first is system initialization, including stack initialization, heap space allocation, interrupt vector table configuration, register initialization, external memory initialization, clock configuration and so on. The second stage is the main program, first of all is to initialize the ARM's ADC module and the I/O port that need to be used in the system, then starts sampling for the radar signal and enables interrupt, stores the sampling data to the specified data buffer. If the sampling points are enough, the FFT transform will be started, and the spectrum of the sampling signal are calculated, then come further analysis and follow-up treatment for the signal spectrum, finally get the velocity. Lastly it is to realize the

control function, namely real-time output and display of the velocity data, speeding alarm and so on.

3.B.1. FFT Algorithm Implementation on the ARM Processor.

FFT algorithm needs to handle a lot of floating-point operations, further more it has high requirements in the multiply-accumulate and data access aspect, while the ARM processor does not support hardware floating-point operations, and there is no single instruction to achieve multiply accumulate And parallel data access. Forasmuch it is necessary to compare FFT's various implementation ways and select a good method.

In the FFT's various implementation ways, we firstly compare the software implementation between the base radix2 DIT Decimation in Time) and radix-4 DITFFT algorithm. Suppose sampling points N=4M (M is a natural number), using radix-2Algorithm needs to multiply MN times, while using radix-4 algorithm requires for 3MN/4 times multiplications, apparently Can save 25% of the multiplication, for the same reason using the radix-8 DIT FFT algorithm can ulteriorly save some multiplications, nevertheless, only 14 registers of S3C2410A can be used, as a result the saving cycles has been consumed by extra load and store. So radix-4 DIT FFT algorithm is the best choice for this core algorithm, and its algorithm process is introduced as follows.

If the length of sequence x(n)is $N=4^n$, it will use following equation to calculate its DFT:

$$x(k) = \sum_{n=0}^{N-1} x(n) w_N^{nk} \qquad k,n = 0,1,2,3,\ldots\ldots N-1 \qquad (4)$$

Radix -4 DIT FFT will break down x(n) in the time domain:

$$x_m(r) = x(4r+m), \quad 0 \le m \le 3, \quad 0 \le r \le \frac{N}{4} - 1. \qquad (5)$$

In the equation: subsequence $x_m(r)$ all are N/4 points sequence. Suppose the DFT of $x_m(r)$ is $x_m(r)$, then:

$$\begin{cases} X(r) = X_0(r) + W_N^r X_1(r) + W_N^{2r} X_2(r) + W_N^{3r} X_3(r) \\ X(r+\frac{N}{4}) = X_0(r) + W_N^{r+\frac{N}{4}} X_1(r) + W_N^{2r+\frac{N}{4}} X_2(r) + W_N^{3r+\frac{N}{4}} X_3(r) \\ X(r+\frac{N}{2}) = X_0(r) + W_N^{r+\frac{N}{2}} X_1(r) + W_N^{2r+\frac{N}{2}} X_2(r) + W_N^{3r+\frac{N}{2}} X_3(r) \\ X(r+\frac{3N}{4}) = X_0(r) + W_N^{r+\frac{3N}{4}} X_1(r) + W_N^{2r+\frac{3N}{4}} X_2(r) + W_N^{3r+\frac{3N}{4}} X_3(r) \end{cases} \qquad (6)$$

In the equation: $0 \le r \le N/4-1$, and because $W^r_N = \exp(-j(2\Pi/N)r)$ then the above equation can be simplified to:

$$\begin{bmatrix} X(r) \\ X(r+\frac{N}{4}) \\ X(r+\frac{N}{2}) \\ X(r+\frac{3N}{4}) \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & -j & -1 & j \\ 1 & -1 & 1 & -1 \\ 1 & j & -1 & j \end{bmatrix} \begin{bmatrix} X_0(r) \\ W_N^r X_1(r) \\ W_N^{2r} X_2(r) \\ W_N^{3r} X_3(r) \end{bmatrix} \qquad (7)$$

From above equation we can get the radix-4 butterfly unit, because the $r=4^{M-1}$ in $X_0(r)$, $X_1(r)$, $X_2(r)$, $X_3(r)$ can continue to break down M-1 times, that is, the whole radix-4 operation totally includes *M* levels, and each level includes N/4 butterfly units. The above amply analyzed FFT algorithms and program structure, but there are still many problems about how to efficiently realize the algorithm on the ARM processor. The following part will introduce some program design features. They greatly improved operational efficiency of the code, and they are the key factors for the system's implementation on the ARM processor as well.

Pipeline Interlock: Execution time of the instruction depends on the pipeline, S3C2410A has 5-stage pipeline, which can concurrently fetch, decode, execute, load memory, and adjust data. If the instruction scheduling is illogical, the current instruction needs result of the previous instruction, but the previous instruction does not finish, then the processor must wait, this is the so-called pipeline interlock. Therefore, this program uses the ARM assembly language to implement algorithms, and carries out the fine-grained control for register allocation and instruction scheduling, thus avoiding pipeline interlock, and greatly improving the operating efficiency.

The Presentation of Floating-point Data: ARM processor does not support floating-point, so this program uses the fixed-point Data to express the floating-point data. This method is based on the requirements of precision in the calculation, which will make the floating-point data left shift, and then use rounding algorithm to reserve the integer part data. In this way the floating-point operations in ARM instructions can be used as part of the four arithmetic operation instructions. It does not take up the Additional instruction cycle, and can greatly improve the efficiency of the code operation.

Data Loading and Storage: When ARM processor is calculating FFT algorithm, it needs to minimize the number of loading and storage times, so that the algorithm can meet the

high performance requirement of the data bandwidth. Therefore, once loaded a data item, it is necessary to use this data item in many operations as possible, you can once calculate multiple outputs, or get multiple operations together, for example, you can simultaneously run a dot product and a signal scale change, while only need loading the data once. Another data storage issue is to divide each complex number into real part and imaginary part to store in a single word, in order to take full advantage of 14 ARM's 32-bit registers.

The Use of Twiddle Factor: In order to improve the computing speed of FFT, calculates the twiddle factor which contains a large number of complex operations beforehand, then uses 14-bit left shift integer data format and divides into real part and imaginary part to store it. Therefore, in the case of the sampling points N =16, 64, 256, 1024, 4096... the twiddle factor can be easily obtained by table look-up approach, not only makes the value of the program's sampling points N optional, moreover it can speed up the computation of the code. Through these innovative design and integration, the radix-4 DIT FFT algorithm flow which finally implemented on ARM processor will be shown in Fig. 5.

4. EXPERIMENT AND TEST RESULT

In order to test the accuracy of the core algorithm, we have produced a sinusoidal signal generator with five-range tuneable frequency, and used this signal as a good pre-treatment radar signals input to the ARM processor, then through the serial port, the Doppler frequency which is calculated by the program will be sent to the PC and displayed on the screen; At the same time, send the calculation value of each sampling points to the PC in order to use these sample values to simulate the corresponding Doppler frequency in MATLAB. The first diagram of Fig. 6 is a sinusoidal signal which is generated by the sinusoidal signal generator, from this diagram we can see that its frequency is 9.2kHz; The second diagram is the spectrum diagram which used output sample value of ARM processor and obtained from simulation in the MATLAB; The third diagram is the enlarged image of the value, from the diagram we can see through this core algorithm, the measured signal frequency is 9182.25Hz. Compare with the true frequency 9.2kHz, the frequency measurement accuracy of this algorithm is very high, which can reach more than 99%. The sampling points N in here are only 256. We can choose N=1024, 4096… in the program, then its frequency measurement accuracy will be higher.

Finally we use this radar velocity-measuring system based on ARM processor to carry out the road test, which is put the radar transceiver front end and the radar signal processing system together to carry out the road test.

The velocity measurement range of this system is 5-250 km/h, and from the test we know this device can detect all type of vehicles, that is to say, it can measure the real-time velocity of trucks, cars, and even bicycles. In addition, the effective measurement distance for the trucks can be up to 1.5km, for the cars also can be up to 1km. Its test results are shown in

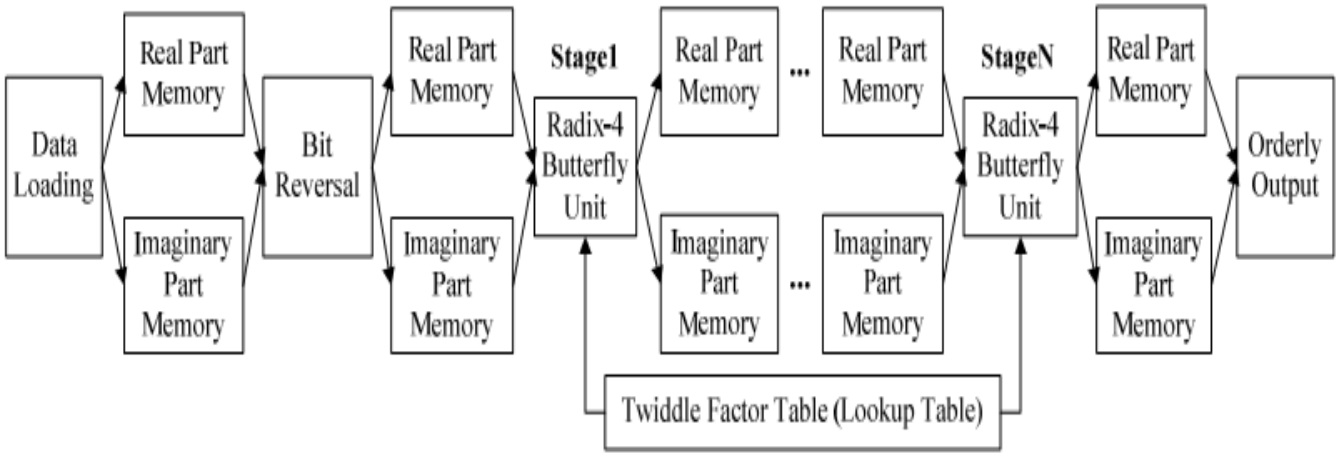

Fig. 5 FFT algorithm flowchart in the ARM

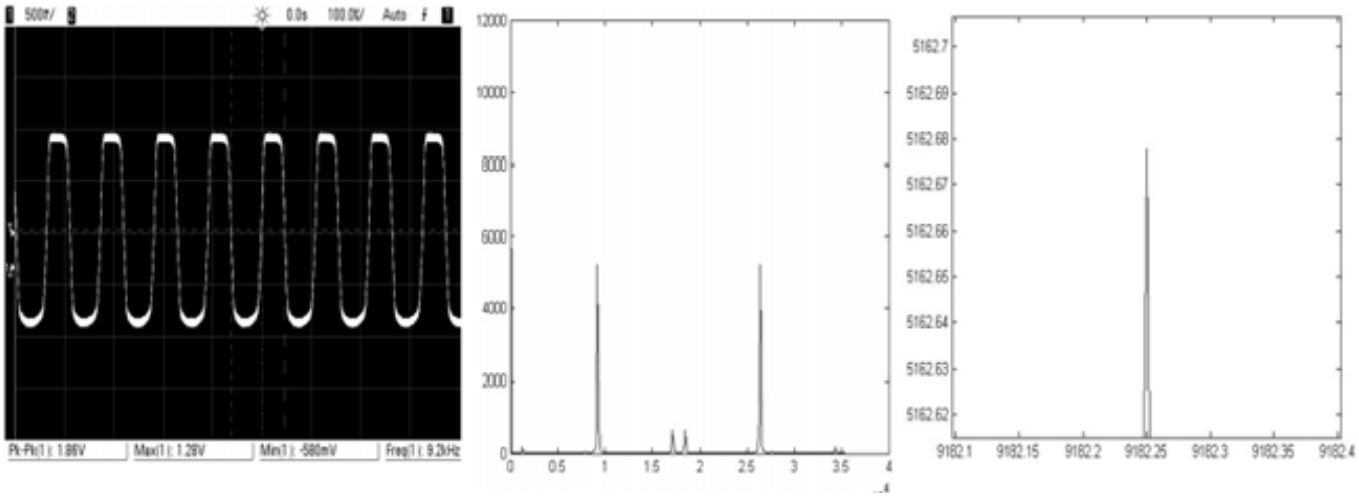

Fig 6: The effect diagram of test

TABLE I. The measured frequency and velocity in the table is the average of 10 times measurements, so we can see its velocity measurement accuracy can reach ±1km/h, which can fully meet the requirements of traffic law enforcement agencies.

TABLE I
ROAD TEST DATA

Real Velocity (km/h)	Measuring Frequency (kHz)	Measuring Velocity (km/h)	Measurement Error (km/h)
30	1.900	29.739	0.261
60	3.810	59.635	0.365
120	7.631	119.442	0.558
150	9.622	150.605	-0.605
180	11.445	179.139	0.861

5. CONCLUSIONS

In order to improve the method of monitoring the velocity of vehicles on road, this paper describes the radar velocity measuring system design and algorithm research based on ARM. The characteristics of this design are reflected by using single-core ARM processor to achieve the dual-core task which is traditionally completed by DSP plus single chip, and It has laid the foundation for ARM's DSP application. The test results show that the accuracy of this system can fully meet. The requirements of traffic law enforcement agencies, and have the advantages of small size, low cost, low power consumption etc. Therefore, it entirely can be applied to traffic management departments in order to enhance the traffic safety.

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