MODELING OF INTERLINE UNIFIED POWER QUALITY CONDITIONER FOR POWER QUALITY DISTURBANCES USING SIMULINK

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Abstract

Proliferation of electronic equipment in commercial and industrial processes has resulted in increasingly sensitive electrical loads to be fed from power distribution system which introduce contamination to voltage and current waveforms at the point of common coupling of industrial loads. The unified power quality conditioner (UPQC) is connected between two different feeders (lines), hence this method of connection of the UPQC is called as Interline UPQC (IUPQC).This paper proposes a new connection for a UPQC to improve the power quality of two feeders in a distribution system. Interline Unified Power Quality Conditioner (IUPQC), specifically aims at the integration of series VSC and Shunt VSC to provide high quality power supply by means of voltage sag/swell compensation, harmonic elimination and power factor correction in a power distribution network, so that improved power quality can be made available at the point of common coupling. The structure, control and capability of the IUPQC are discussed in this paper. The efficiency of the proposed configuration has been verified through simulation using MATLAB/ SIMULINK.

Index terms*: Distribution system, Interline unified power quality conditioner (IUPQC), power quality, pwm technique, sensitive load, voltage sag, voltage swell and voltage source converter.*

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1. INTRODUCTION

Power Electronics has three faces in power distribution, first one that introduces valuable industrial and domestic equipment, a second one that creates problems and finally a third one that helps to solve those problems. Modern semiconductor switching devices are being utilized more and more in a wide range of applications in distribution networks, particularly in domestic and industrial loads. Examples of such applications widely used are Adjustable Speed motor Drives (ASD's), Diode and Thyristor rectifiers, Uninterruptible Power Supplies (UPS), computers and their peripherals, consumer electronics appliances (TV sets for example) and arc furnaces. Complications related to the use of non-linear loads for these systems have been a major issue for a long time for both power providers and users alike. Power problems are partially solved with the help of LC passive filters.

However, this kind of filter cannot solve random variations in the load current waveform. They also can produce series and parallel resonance with source impedance. To solve these problems, shunt active power filters have been developed, which are widely investigated today. These filters work as current sources, connected in parallel with the nonlinear load, generating the harmonic currents the load requires. A Unified Power Quality Conditioner (UPQC) can perform the functions of both DSTATCOM and DVR. The UPQC consists of two Voltage-Source Converters (VSCs) that are connected to a common DC bus. One of the VSCs is connected in series with a distribution feeder, while the other one is connected in shunt with the same feeder. The DC links of both VSCs are supplied through a common DC capacitor.

1.1Basic types of loads

1. Unbalanced loads*:* The loads connected to the line are said to unbalanced if they draw the currents which are not in the phase difference as source voltage

2. Non linear load*:* The most common linear loads in power electronics system are resistors, inductors and capacitors. The most common nonlinear loads are diode rectifier, thyrisitor chopper, arc furnace, and switching mode power supply. A linear load could be defined as a linear relationship between the voltage across and the current through the load or their derivatives. Although there is no explicit mathematical description for nonlinear loads, they could be described as "a load that draws a non-sinusoidal current wave when supplied by a sinusoidal voltage source".

3. Sensitive load*:* The load which will be readily respond to the disturbances even for small duration and will effected early towards the non linearity in the system. Hence we have to keep the load with better safety measures.

2. SYSTEM DESCRIPTION

2.1 Proposed Configuration

The single-line diagram of an IUPQC [7] connected distribution system is shown in Fig.1 Two feeders, Feeder-1 and Feeder-2, which are connected to two different substations; supply the system loads L-1 and L-2. The supply voltages are denoted by V_{s1} and V_{s2}. It is assumed that the IUPQC is connected to two buses B-1 and B-2, the voltages of which are denoted by V_{t1} and V_{t2}, respectively. Further two feeder currents are denoted by i_{s1} and i_{s2} while the load currents are denoted by i_{l1} and i_{l2}. The load L-2 voltage is denoted by $V_{l2.}$ The purpose of the IUPQC is to hold the voltages V_{t1} and V_{l2} constant against voltage sag/swell, temporary interruption and momentary interruption etc. in either of the two feeders. It has been demonstrated that the IUPQC can absorb power from one feeder (say feeder-1) to hold V_{l2} constant in case of a sag in the voltage V_{s1}. This can be accomplished as the two VSCs are supplied by a common dc capacitor. The dc capacitor voltage control has been discussed here along with voltage reference generation strategy. Also, the limits of achievable performance have been computed. The performance of the IUPQC has been evaluated through simulation studies using MATLAB/SIMULINK.

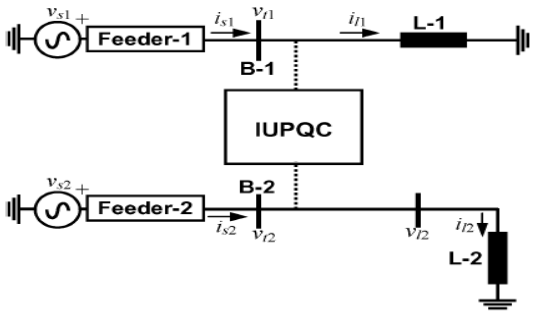

Fig.1 Single-line diagram of an IUPQC-connected distribution system.

Basically IUPQC is the device UPQC kept in between two individual feeders, (called feeder-1 and feeder-2). UPQC consists of two back to back connected MOSFET based voltage source bi-directional converters or Voltage Source Converters (VSCs) (called VSC-1 and VSC-2) with a common DC bus. VSC-1 is connected in shunt with feeder-1 while VSC-2 is placed in series with the feeder-2.

The complete structure of a three-phase IUPQC with two such VSCs is shown in Fig.2 The secondary (distribution) sides of the shunt-connected transformers (VSC-1) are connected in star with the neutral point being connected to the load neutral. The secondary winding of the series-connected transformers (VSC-2) are directly connected in series with the bus B-2 and load L-2. The AC filter capacitors C_f and C_k are also connected in each phase Fig.2 to prevent the flow of the harmonic currents generated due to switching. The six inverters of the IUPQC are controlled independently.

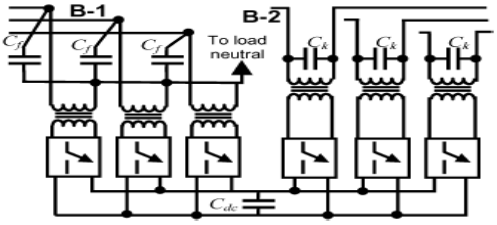

Fig.2 Complete structure of an IUPQC.

An IUPQC connected to a distribution system is shown in Fig.3. In this Figure, the feeder impedances are denoted by the pairs ($R_{s1,}$ L_{s1}) and ($R_{s2,}$ L_{s2}). It can be seen that the two feeders supply the loads L-1 and L-2. The load L-1 is assumed to have two separate components as unbalanced part (L-11) and a non-linear part (L-12). The currents drawn by these two loads are denoted by i_{l11} and i_{l12}, respectively. We further assume that the load L-2 is a sensitive load that requires uninterrupted and regulated voltage. The length of Feeder-1 is arbitrarily chosen to be twice that of Feeder-2.

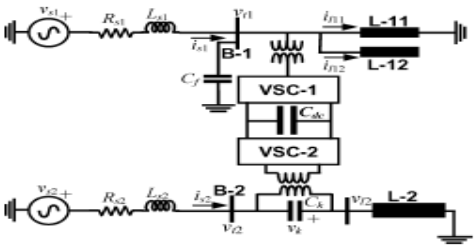

Fig. 3 Typical IUPQC connected in a distribution system.

2.2. Voltage Source Converter

The schematic structure [5] of a VSC is shown in Fig.4 In this structure; each switch represents a power semiconductor device (e.g., IGBT) and an anti-parallel diode as shown in Fig.4. The main objective of static power converters is to produce an ac output waveform from a dc power supply.

These are the types of waveforms required in adjustable speed drives (ASDs), uninterruptible power supplies (UPS), static var compensators, active filters, flexible ac transmission systems (FACTS), and voltage compensators, which are only a few applications.

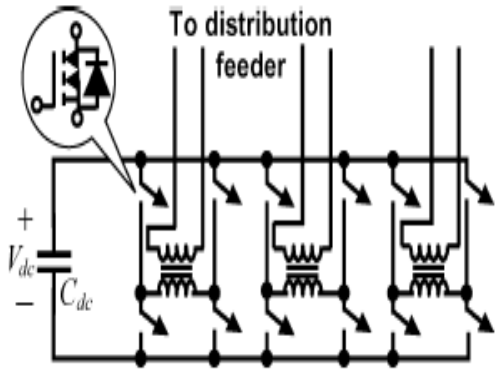

Fig.4 Schematic structure of a VSC.

The main objective of static power converters is to produce an ac output waveform from a dc power supply. These are the types of waveforms required in adjustable speed drives (ASDs), uninterruptible power supplies (UPS), static var compensators, active filters, flexible ac transmission systems (FACTS),[1] and voltage compensators, which are only a few applications.

The length of Feeder-1 is arbitrarily chosen to be twice that of Feeder-2. The voltage of bus B-1 and load L-1 currents, when no IUPQC is connected to the distribution system, are shown in Fig. 5. In this figure and in all the remaining figures showing three phase waveforms, the phases a, b and c are depicted by solid, dashed and dotted lines, respectively. It can be seen from Fig. 5(a), that due to the presence of unbalanced and non-linear load L-1, the voltage is both unbalanced and distorted. Also, the load L-11 causes an unbalance in the current, while load L-12 causes distortion in the current .We shall now demonstrate how these waveforms can be improved using the IUPQC.

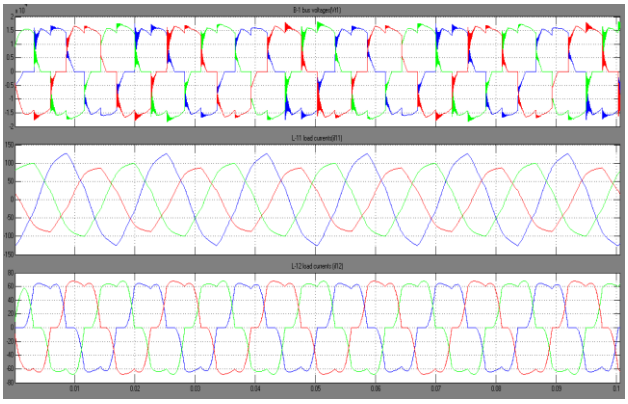

Fig.5 Simulation results – in absence of IUPQC: a)B-1 bus voltages (V_{t1}),KV, (b) L-11 load currents (i_{l11}),A and (c) L-12 load currents (i_{l12}),A.

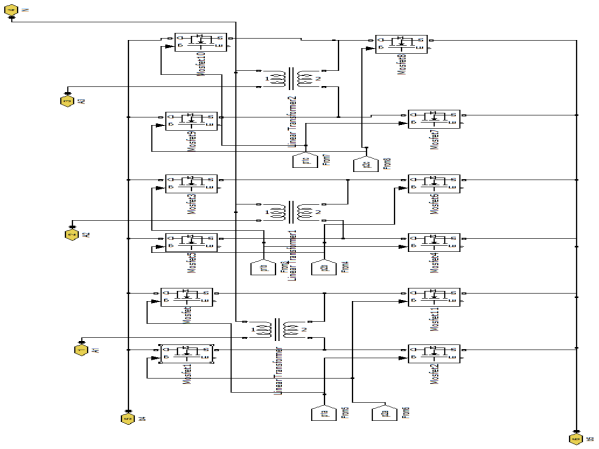

Fig. 6 Shunt control block (subsystem)

Simulink designed circuit for the shunt VSC of IUPQC is shown in fig.6 consists of twelve MOSFET switches four of each connected to one phase. PWM controller(8) will generate two type of pulses for each phase, two valves will operate simultaneously with each pulse like valves[2,12] for one pulse & valves[1,11] of a limb of phase a. Each valve closes for 180^0 and a new valves is triggered after every 60^0.the operation series block will also be same as that of shunt.

Here each phase separately given with a 1-phase transformer to reduce the harmonics and simplified Simulink design. The reason for the use of MOSFET in the design is due to its high operating frequency up to 1 MHz, and available voltage & current ratings are upto 500V, 140A, where as IGBT can be operated only up to 50 KHz.

3. GENERATION OF GATING SIGNALS

3.1. Control Strategy for IUPQC

Control objective of DVR is to mitigate voltage sag[2] and that of active filters is to mitigate harmonics, whereas UPQC can take care of different power quality disturbances like sag, swell, flicker, spike, harmonics, impulsive transient and momentary interruption. The important issues in the design of the control strategy are the generation of reference currents/voltages for compensation and the generation of the compensating current/voltage based on the reference currents/voltages.

3.2 Series control: The series inverter, which is operated in current control mode, isolates the load from the supply by introducing a voltage source in between. This voltage source compensates supply voltage deviations such as sag and swell. The three phase reference voltages (V_{la}^*, V_{lb}^*,V_{lc}^*) are generated by subtracting the three phase load voltage (V_{la},V_{lb},V_{lc}) from three phase supply voltages (V_{sa},V_{sb},V_{sc}). In closed loop control scheme of the series inverter, the three phase load voltages (V_{la},$V_{lb,}V_{lc}$) are subtracted from the three phase supply voltages (V_{sa}, V_{sb}, V_{sc}), and are also compared with reference supply voltage which results in three phase reference voltages (V_{la}^*,V_{lb}^*,V_{lc}^*). These reference voltages are to be injected in series with the load.The series inverter acts as a load to the common DC link (provided by a capacitor) between the two inverters. When sag occurs series inverter exhausts the energy of the DC link.

The impedance Z_{se} includes the impedance of insertion transformer. The currents (i_{sea}^*, i_{seb}^*, i_{sec}^*) are ideal current to be maintained through the secondary winding of insertion transformer in order to inject voltages (V_{la},$V_{lb,}V_{lc}$), thereby accomplishing the desired task of compensation of the voltage sag. The currents I_{ref} (i_{sea}^*,i_{seb}^*,i_{sec}^*) are compared with I_{act} (i_{sea}, i_{seb}, i_{sec}) in PWM current controller. As a result six switching signals are obtained for the MOSFETs of the series inverter as shown in Fig7 the firing signals enable the series inverter to generate the required injection voltage.

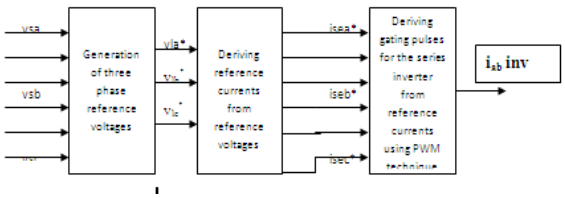

Fig.7 Generation of gating signal

3.3. Shunt Control*:* Shunt control is used to inject compensating currents to eliminate harmonics at the load end and also charge the capacitor to the required value to drive the VSC. This involves generation of the required compensating currents

3.4 Generation of compensating current: There are two methods for finding compensating current. They are direct method and indirect method. The direct method is used in the present study.The output I_{sp} is considered as magnitude of three phase reference currents. Three phase unit current vectors ($U_{sa,}U_{sb,}U_{sc}$) are derived in phase with the three phase supply voltages (V_{sa}, V_{sb}, V_{sc}). These unit current vectors (U_{sa} ,U_{sb} ,U_{sc}) form the phases of three phase reference currents. Multiplication of magnitude i_{sp} with phases (U_{sa} ,U_{sb} ,U_{sc}) results in the three phase reference supply currents (i_{sa}^*, i_{sb}^*, i_{sc}^*).Subtraction of load currents (i_{la}^*,i_{lb}^*,i_{lc}^*) from the reference supply currents (i_{sa}^*,i_{sb}^*,i_{sc}^*) results in three phase reference currents (i_{sha}^*, i_{shb}^*, i_{shc}^*) for the shunt inverter. These reference currents I_{ref} (i_{sha}^*,i_{shb}^*,i_{shc}^*) are compared with actual shunt currents I_{act} (i_{sha},i_{shb},i_{shc}) and the error signals are then converted into (or processed to give) switching pulses using PWM technique which are further used to drive shunt inverter. In response to the PWM gating signals the shunt inverter supplies harmonic currents required by load

3.5. PI Controller

The Proportional Integral (PI) controller compares the DC capacitor voltage[7] with reference DC capacitor voltage which in turn generates the current $I_{sp,}$ is considered as magnitude of three phase reference currents is given to the three-phase reference current generation block. The three-phase reference current generation block computes the unit vectors, three phase reference supply currents and the shunt current references. The output of the PWM current controller gives the necessary gating signals to drive the shunt VSC to generate the required compensating currents. The PI controller processes the error signal and generates the required angle δ to drive the error to zero, in example; the load rms voltage is brought back to the reference voltage. In the PWM generators, the sinusoidal signal, $v_{control}$, is phase modulated by means of the angle δ or delta the modulated signal, $v_{control}$ is compared against a triangular signal (carrier) in order to generate the switching signals of the VSC valves.

System Quantities	Values
System fundamental frequency	50Hz
Voltage source V_{s1}	11kv(L-L,rms), phase angle 0^0
Voltage source V_{s2}	11kv(L-L,rms), phase angle 0^0
Feeder-1 (R_{s1} + j2∏fL_{s1})	Impedance:6.05+j36.28Ω
Feeder-2 (R_{s2} + j2∏fL_{s2})	Impedance:3.05+j18.14Ω
Load L-11 Unbalanced RL component	Phase a: 24.2+j60.50Ω Phase b: 36.2+j78.54 Ω Phase b: 48.2+j94.25 Ω
Load L-12 Non-linear component	A three-phase diode rectifier that Supplies a load of 250+j31.42Ω
Balanced load L-2 Impedance	72.6+j54.44 Ω

TABLE I SYSTEM PARAMETERS

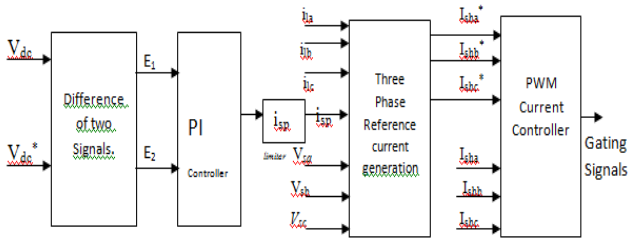

Fig .8 Block diagram for generation of gating signals

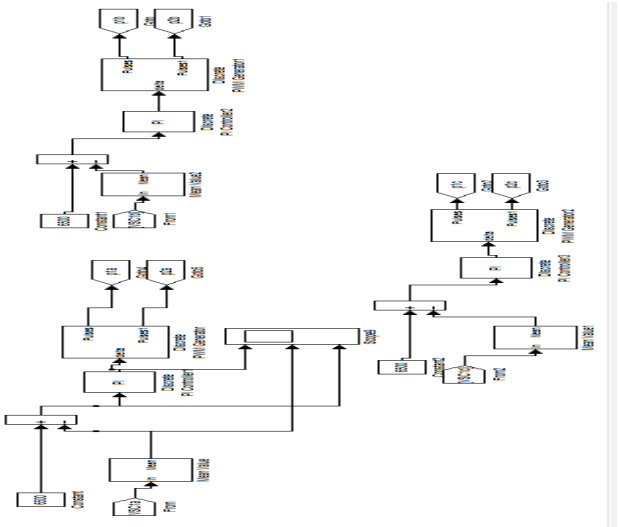

Fig.9 PWM current controller (subsystem)

A PWM generator shown in fig8.consists of a comparator which takes the value of delta (δ) from PI controller and compares with a reference value, its output is given to Boolean function and through logic gates two pulses will generate which complement to each with NOT gate. As mentioned earlier each pulse will operate two valves in at a time in phase.

4. DESIGN CONSIDERATIONS

4.1 .Calculation Of Dc Capacitor (Cdc) And Filter Capacitors (Cf & Ck)

As the DC capacitor is used for back up energy storing device during the fault conditions. The value of DC capacitor will be taken by considering the maximum value of power supplied by it. During L-L-L-G fault the capacitor should supply maximum power i.e. the total power supplied by three phase.

Total 3-phase power = $\sqrt{3}\ V_L\ I_{L\ COS\Phi} = 1.09$ MW

Where V_L = line to line voltage = 11KV

I_L = current through the feeder= V_L/Z_{S2}

CosΦ= power factor and

$\Phi = \tan^{-1}[X_{s2} / R_{S2}] = \tan^{-1}[30.73/3.07] = 81.2^0$

During 3-phase fault the capacitor voltage falls below 2KV.

Power supplied by capacitor C is $V_{DC}\ I_{DC}$= 1.09 MW.

$(V_{DC})^2/Z_{dc}$=1.09M

$1/2\prod fc_{DC})=1.09M/(V_{DC})^2$ {V_{DC} Assumed as 1.6KV}

From the above taking the value of V_{dc} below 2KV

We get DC capacitor value [8] approximately C_{dc}= 3000µF.

Filter capacitors C_f and C_k are used to reduce the harmonics present in ac supply given to the bus. Generally the filter impedance value should such that it must show a high impedance path for the respective harmonics to be reduced. On ac side 3rd harmonics are frequently present, as C_f is connected in shunt with feeder-1 and C_k in series with feeder-2, the shunt connected capacitor(C_f) to feeder-1 should show minimum impedance to the harmonics.

Also series capacitor connected to feeder-2 should show maximum impedance to the harmonics.

With above criteria the values may in the range of

C_f >20 µf and C_k <50 µf

SYSTEM QUANTITIES	PARAMETERS
System fundamental frequency	50Hz
VSC-1 Single phase transformer	1MVA,3/11kv 10% leakage reactance
VSC-2 Single phase transformer	1MVA,3/11kv 10% leakage reactance
Filter capacitor (C_f)	50μf
ilter capacitor (C_k)	30μf
DC capacitor (C_{dc})	3000 μf

TABLE 2 IUPQC PARAMETERS

4.2. Theoretical Analysis

IUPQC Operation*:* As mentioned before, the shunt VSC (VSC-1) holds the voltage of bus B-1 constant. This is accomplished by making the VSC-1 to track a reference voltage across the filter capacitor C_f. The equivalent circuit of the VSC-1 is shown in Fig 8 in which u_1V_{dc} denote the inverter output voltage where V_{dc} is dc capacitor voltage and u_1 is switching action equal to where $\pm n_1$ is turns ratio of the transformers of VSC-1. In fig.8 the inverter losses and leakage inductance of the transformers are denoted by R_{f1} and L_{f1}, respectively. All system parameters are referred to the line side of the transformers.

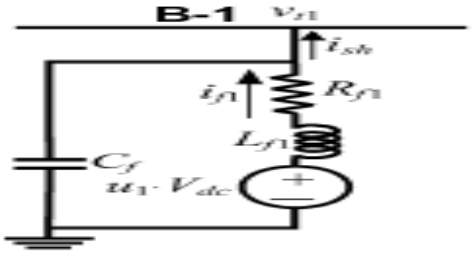

Fig .10 the equivalent circuit of the VSC-1

Defining the state vector as,

$$X_1^T = [V_{t1}\ i_{f1}] \quad (1)$$

The state space model for the VSC-1 is written as

$$\dot{x}_1 = F_1 x_1 + G_1 z_1$$

$$Y_1 = V_{t1} = Hx_1 \quad (2)$$

Where

$$z_1 = \begin{pmatrix} u_{1c} \\ i_{sh} \end{pmatrix} \qquad H = [1\ 0] \qquad G_1 = \begin{pmatrix} 0 & \frac{1}{C_f} \\ -\frac{V_{dc}}{L_{f1}} & 0 \end{pmatrix}$$

Note that u_{1c} is the continuous time equivalent of u_1. The system given in fig.10 is discredited and is written in input–output form as

$$A_1(z^{-1})Y_1(k) = B_1(z^{-1})\, u_{1c}(k) + C_1(z^{-1})\, \eta_1(k) \quad (3)$$

Where η_1 is a disturbance which is equal to i_{sh}.

The reference $y_{1ref}(k)$ is the desired voltage of the bus B-1. The peak of this instantaneous voltage is pre-specified and its phase angle δ_1 is adjusted to maintain the power balance in the system. To set the phase angle, we note that the dc capacitor must be able to supply VSC-1 while maintaining its dc bus voltage constant by drawing power from the ac system.

A proportional controller is used for controlling the dc capacitor voltage and is given by

$$\delta_1 = K_p\,(V_{davg} - V_{dref}) \quad (4)$$

Where V_{dcav} is the average voltage across the dc capacitor over a cycle, V_{dcref} is its set reference value and K_p is the proportional gain. It is to be noted that the average voltage V_{dcav} is obtained using a moving average low pass filter to eliminate all switching components from the signal. The equivalent circuit of the VSC-2 is shown in Fig. 11 and is similar to the one shown in Fig. 10 in every respect

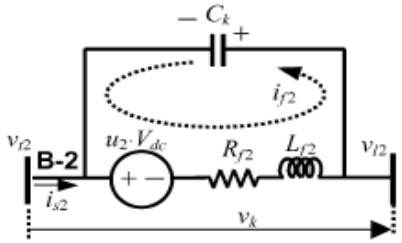

Fig.11 The equivalent circuit of the VSC-2

Defining a state and input vector, respectively, as

$$X_2^T = [V_{t2}\ i_{f2}] \quad (5)$$

And the state space model for VSC-2 is given as

$$\dot{x}_2 = F_2 x_2 + G_2 z_2$$

$$Y_2 = V_{t2} = Hx_2 \quad (6)$$

Where F_2 and G_2 and are matrices that are similar to F_1 and G_1 , respectively. The discrete-time input–output equivalent of fig. 11 is given as

$$A_2(z^{-1})Y_2(k) = B_2(z^{-1})\, u_{2c}(k) + C_2(z^{-1})\, \eta_2(k) \quad (7)$$

Where η_2 is a disturbance which is equal to i_{sh2}.

Note from fig.11 that the purpose of the VSC-2 is to hold the voltage V_{l2} across the sensitive load L-2 constant. Let us denote

the reference load L-2 voltage as V^*_{l2}.
Then the reference y_{2ref} is computed by the application of Kirchhoff's voltage law as

$$Y_{2\,ref} = V_{l2}^* - V_{t2} \quad (8)$$

The peak of the reference voltage y_{1ref} is chosen as 9KV and its angle is computed from the angle controller (4) with K_p= -0.25. The reference voltage V^*_{l2} is chosen as a sinusoidal waveform with a peak of 9KV and a phase angle of -10°.

4.3 Performance with IUPQC

It is assumed that the dc capacitor is initially uncharged and both the feeders along with the IUPQC [9] are connected at time zero. It can be seen from fig.12, that the three-phase B-1 voltages V_{t1}, are perfectly balanced with a peak of 9 KV. Once these voltages become balanced, the currents drawn by feeder-1, i_{s1}, also become balanced. The load L-2 bus voltages V_{t2}, shown in fig.12 are also perfectly sinusoidal with the desired peak of (9 KV) as the converter VSC-2 injects the required voltages in the system. The bus B-2 voltages, .The dc capacitor voltage V_{dc} is shown in Fig.13. It can be observed that it has a settling time of about 4 cycles (0.08 s) and it attains a steady-state value of about 4.17 KV.

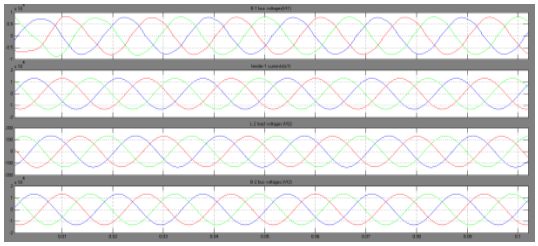

Fig.12 System performance with an IUPQC. (a)B-1 bus voltages (V_{t1}),KV, (b) Feeder-1 currents (i_{s1}),A, (c) L-2 load voltages (V_{l2}),KV, (d) B-2 bus voltages (V_{t2}),KV.

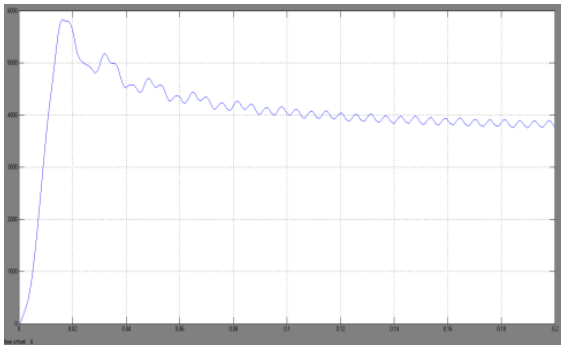

Fig.13 DC capacitor voltage (V_{dc}), KV

5. PERFORMANCE EVALUATIONS

The performance of IUPQC has been evaluated considering various disturbance conditions:
a) Unbalance due to disturbance in Voltage in the feeders (sag, swell).
b) Upstream fault in feeder (L-G, L-L-G, 3-Ø to ground).
c) Unbalance due to Load change.

5.1. Voltage Sag in Feeder-1

As sag [9] is a temporary drop, it is turn ON and turn OFF by circuit breaker for a time period of 0.15s to 0.25s in which peak of the supply voltage V_{s1}, reduces to 6.5 KV from their nominal value of 9 KV.

The various waveforms of only one phase (phase-a) are shown in Fig. 14 the trends in the other two phases are similar. It can be seen that the dc capacitor voltage V_{dc}, drops as soon as the sag occurs. If the bus voltage remains constant, the load power also remains constant. However, since the source voltage V_{s1} has dropped, the power coming out of the source has reduced. In order to supply the balance power requirement of the load, the V_{dc} drops. To offset this, the angle δ_1 retards such that the power supplied by the source increases. As the sag is removed, both the voltage V_{dc} and phase angle δ_1 returns to their steady state values. The current through feeder-1 is also shown in Fig.14. It can be seen that in order to supply the same load power at a reduced source voltage, the feeder current increases. Also, the transients in this current occur at the inception and the removal of the sag due to change in the source voltage.

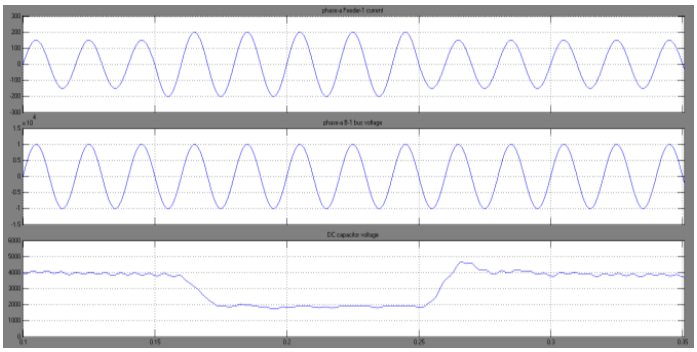

Fig.14 System response during voltage sag in Feeder-1: (a) phase-a Feeder-1 current, A, (b) phase-a B-1 bus voltage, KV, (c) DC capacitor voltage (V_{dc}), KV.

5.2 Performance limits: Let us assume the following phasor voltages

$$V_{s1} = V_1\angle 0^0 \text{ and } V_{t1} = V_2\angle\delta_1 \quad (9)$$

Then the current flowing through Feeder-1 is

$$I_{s1} = \frac{V_1\angle 0^0 - V_2\angle\delta_1}{R_{s1} + jX_{s1}} \quad (10)$$

Where $X_{s1}= \omega L_{s1}$,

ω-being the system fundamental frequency in rad/s.

Therefore, the per phase real power entering bus B-1 is given by

$P_{t1}=Re\{V_{t1}^* I_{s1}\}=Re\{V_2\angle \delta 1 \left(\frac{V_1\angle o^0 - V_2\angle\delta_1}{R_{s1} + jX_{s1}}\right)\}$

$$= \frac{1}{R_{s1}^2 + X_{s1}^2}\left[(V_1V_2\cos\delta_1 - V_2^2)R_{s1} - V_1V_2 X_{s1}\sin\delta_1\right]$$

Solving for δ_1 from the above equation, we get

$$R_{s1}\cos\delta_1 - X_{s1}\sin\delta_1 = \frac{P_{t1}(R_{s1}^2 + X_{s1}^2) + V_2^2 R_{s1}^2}{V_1V_2}. \quad (11)$$

Above Equation forms the basis for the computation of the performance limit. Let us assume that both the VSCs are lossless (i.e., average power entering the bus B-1 is entirely consumed by the load L-1). It is additionally assumed that the power consumed by load L-2 is entirely supplied by the source V_{s2}. Then as V_2 is held constant, the power consumed by the load, and hence P_{t1}, will remain constant. Therefore, the right hand side of (11) is a constant for a particular value of source voltage V_1.

Let us denote this constant as γ, that is

$$\gamma = \frac{P_{t1}(R_{s1}^2 + X_{s1}^2) + V_2^2 R_{s1}^2}{V_1V_2} \quad (12)$$

Also, let us define the feeder impedance as

$$Z_{s1}=R_{s1}+jx_{s1}= \sqrt{R_{s1}^2 + X_{s1}^2} = |Z_{s1}|\angle\varphi_1$$

Such that feeder resistance and reactance can be written as

$$R_{s1}= |Z_{s1}|\cos\varphi_1 \text{ and } X_{S1}=|Z_{s1}|\sin\varphi_1$$

Therefore, δ_1 from (11) can be written as

$$\delta_1=\cos^{-1}\left(\frac{\gamma}{|Z_{s1}|}\right) - \varphi_1 \quad (13)$$

For the system data given in Tables 1 and 2, the average three-phase real power drawn by the load L-1 for a line-to-line bus B-1 voltage of 11 KV, is 1.47 MW. Since the bus B-1 voltage is balanced, this power is supplied equally by all the three phases. Therefore, we choose P_{t1} as 0.49 MW. The values of δ_1 calculated from (13) and that obtained through simulation for different levels of voltage sag in V_{s1} are listed in Table 3from this table, it can be observed that there is a small discrepancy between the calculated and simulated values of δ_1.

This discrepancy increases as the amount of sag increases. The derivation of (14) assumes that the VSCs are lossless. In practice, however, the losses in VSC-1 and VSC-2 are drawn from the ac system by the angle controller .This implies that an additional amount of real power is entering bus B-1 and hence P_{t1} is equal to power supplied to the load L-1 plus the losses in the VSCs. In Table 3, the simulation fails when the source voltage drops to 5.75 KV.

The calculated value of δ_1 is -63.27° for this case and the ac system fails to provide the additional power required to replenish the VSC losses. As a consequence, the dc capacitor voltage collapses. It is to be noted that will produce real solution so long as the following condition is satisfied:

$$\gamma \le |Z_{s1}| \quad (14)$$

When γ is equal to $|Z_{s1}|$, δ_1 becomes equal to $-\varphi_1$, which is -80.53°. Therefore, if the source voltage drops even to 5.49 KV, (14) gets violated. This problem can be solved by either reducing the load L-1 or by reducing the reference magnitude of the bus B-1 voltage V_2. In both of these cases P_{t1}, reduces, ensuring that (13) is satisfied. For example, if the load is made to be 80% of the nominal value, then the angle δ_1 calculated from (13), is -60.19° for peak of V_{s1} being 5.0 KV.

Peak of V_{s1} =1.414V_1(KV)	Value of δ_1 (deg)	
	Calculated from 23	Obtained from simulation
9.0	-28.22	-33.88
8.5	-30.77	-36.92
8.0	-30.88	-40.72
7.5	-37.60	-45.70
7.0	-42.20	52.81
6.5	-48.18	-57.36
6.0	-56.76	-61.22

5.75	-63.27	-
5.5	-77.25	-

TABLE 3 VARIATIONS IN VOLTAGE ANGLE WITH SAG

5.3. Upstream Faults In Feeder-2(L-G, L-L-G, 3-Ø To Ground)

1. L-G fault: The performance of the IUPQC is tested, when a L-G fault occurs in Feeder-2 at bus B-2. Phase- a is effected fault with ground for a time interval of 0.15s to 0.35s which is turn-ON and turn-OFF by using circuit breaker.

The below waveform shows when L-G fault [7] occurs at 0.15s, such that the a-phase of B-2 bus voltage becomes zero. When the fault occurs, the power fed to load L-2 by Feeder-2 is reduced. To meet the power requirement of the load L-2, the dc capacitor starts supplying this power momentarily. This causes the dc capacitor voltage to drop from 3.8 KV to 2.7 KV. It can be seen from Fig14 that the L-2 load voltages remain balanced throughout the fault period.

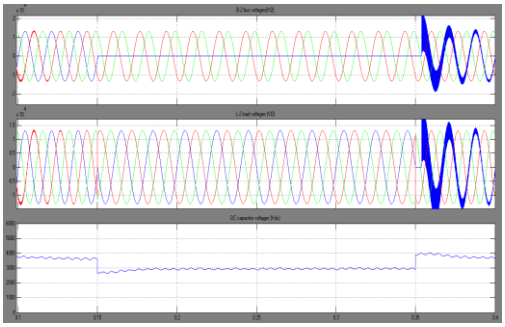

Fig.14. System response during L-G fault at bus B-2: (a) B-2 bus voltages (V_{t2}), KV, (b) L-2 load voltages (V_{l2}),KV, (c) DC capacitor voltage *(V_{dc}),KV.*

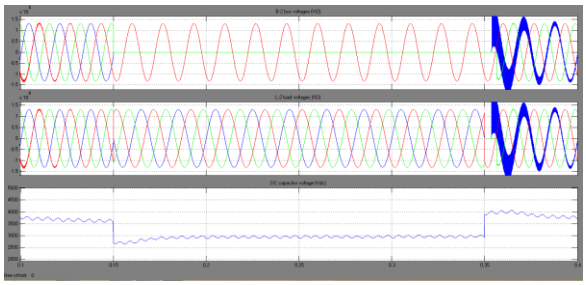

Fig.15 System response during L-L-G fault at bus B-2: (a) B-2 bus voltages (V_{t2}), KV, (b) L-2 load voltages (V_{l2}), KV, (c) DC capacitor voltage (V_{dc}),KV.

2. L-L-G fault The above waveforms shows when a 10 cycle L-G fault occurs at 0.15s such that both the a and b-phases of B-2 bus voltage become zero. B-2 bus voltages are shown in Fig.15 (a). It can be seen from Fig.15 (b) that the L-2 load voltages remain balanced. However, the dc capacitor voltage now drops from 3.75KV to 2.65 KV. Still it is enough to regulate both the load voltages.

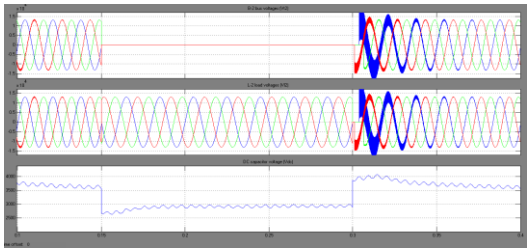

Fig.16. System response during L-L-L-G fault at bus B-2: (a) B-2 bus voltages (V_{t2}), KV, (b) L-2 load voltages (V_{l2}),KV, (c) DC capacitor voltage (V_{dc}),KV.

3. L-L-G fault: The fig.16 Waveform shows when L-L-L-G fault occurs at 0.15s, such that all 3-phases of B-2 bus voltage become zero. When the fault occurs, the power fed to load L-2 by Feeder-2 is reduced. To meet the power requirement of the load L-2, the dc capacitor starts supplying this power momentarily. This causes the dc capacitor voltage to drop from 3.8 KV to 2.7 KV. It can be seen from Fig.16 (b), that the L-2 load voltages remain balanced throughout the fault period.

4. Load change: Here to produce change in load, the unbalanced RL load L-11 is doubled by reducing its unbalanced impedances to half at 0.15s, it is turn on and turn off by circuit breaker for a time period of 0.15s to 0.25s.

The nonlinear load L-12, however, has been kept unchanged. The system response is shown in Fig.17. It can be seen that as the load increases, the dc link voltage reduce and attain a new steady state. However, the bus B-1 voltage remains undisturbed.

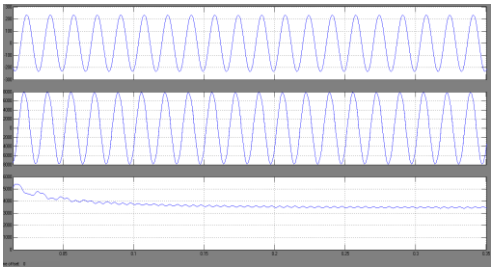

Fig.17 System response during the change in load L-11: (a) phase-a B-1 bus voltage,KV, (b) phase-a L-1 load current, A, (c) DC capacitor voltage (V_{dc}),KV.

CONCLUSION

The paper illustrates the operation and control of an Interline unified power quality conditioner (IUPQC). The device is connected between two feeders coming from different substations. An unbalanced and non-linear load L-1 is supplied by feeder-1 while a sensitive load L-2 is supplied through feeder-2. The main aim of the IUPQC is to regulate the voltage at the terminals of feeder-1 and to protect the sensitive load from disturbances occurring upstream. The performance of the IUPQC has been evaluated under various disturbance conditions such as voltage sag in either feeder, fault in one of the feeders and load change. It has been shown that in case of voltage sag, the phase angle of the bus voltage in which the shunt VSC is connected plays an important role as it gives the measure of the real power required by the load. The IUPQC can mitigate voltage sag [9] of about 9 KV to 5.5 KV in Feeder-1 and 9 KV to 3 KV in Feeder-2 for short duration. The IUPQC in the paper is capable of handling system in which the loads are unbalanced and distorted. Extensive case studies have been included to show that an IUPQC might be used as a versatile device for improving the power quality in an interconnected distribution system. The IUPQC has been shown to compensate for several of these events successfully.

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