A VERSATILE APPROACH TO DESIGN AND IMPLEMENT A FOOLPROOF SECURITY SYSTEM USING INERTIAL MICROMACHINED SENSOR

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Abstract
In this paper we present a Wireless security system for electronic equipments using inertial MEMS sensor which is implemented using an embedded microcontroller. Equipment security is an emerging field in the today's electronic world. Securing sensitive electronic equipments and expensive equipments have become vital these days due to increased number of thefts. Especially when the sensitive equipment is stored and accessed via networked environment, considerable attention must be taken to ensure equipments are not accessed by unauthorized users. To safeguard the equipments, an intelligent system can be designed using microcontroller along with a MEMS sensor to detect the physical displacement of the equipment. By getting an external interrupt when unauthorized person try to access the device the system would alarm and will alert the owners to detect the theft. Since this system is useful to detect and avoid thefts, it is also called as Anti theft system. In this paper we have proposed a method using MEMS sensor and a micro controller for protecting electronic equipments (which are operating from remote locations) from the intruder and transfer the message instantaneously to the authorised person.

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1. INTRODUCTION

Micro-electro mechanical systems or MEMS are integrated micro devices or systems combining electrical and mechanical components. They are fabricated using integrated circuit(IC) batch processing techniques and can range in size from micrometers to milli-meters. These systems can sense control and actuate on the micro scale and function individually or in arrays to generate effects on the micro scale.

The field of micro electro mechanical system (MEMS) is based on the use of integrated circuit (IC) fabrication techniques to create devices capable of acting as mechanical, electrical, and chemical transducers for applications in areas such as automotive and medical industries.

It can be difficult for one to imagine the size of MEMS device. The general size of MEMS is on the order of microns (10 power -6 meter). The main characteristic of MEMS is their small size. Due to their size, MEMS cannot be seen with the unaided eye. An optical microscope is usually required for one to be able to see them.

2.TYPICAL APPLICATIONS

•HDD MP3 Player: Freefall Detection
•Laptop PC: Freefall Detection, Anti-Theft
• Cell Phone: Image Stability, Text Scroll, Motion Dialing, E-Compass
• Pedometer: Motion Sensing
• PDA: Text Scroll
• Navigation and Dead Reckoning: E-Compass Tilt Compensation
• Gaming: Tilt and Motion Sensing, Event - Recorder
• Robotics: Motion Sensing

3.FUNCTIONAL BLOCK- DIAGRAM OF THE SYSTEM

The functional block diagram for implementing the system is as shown.

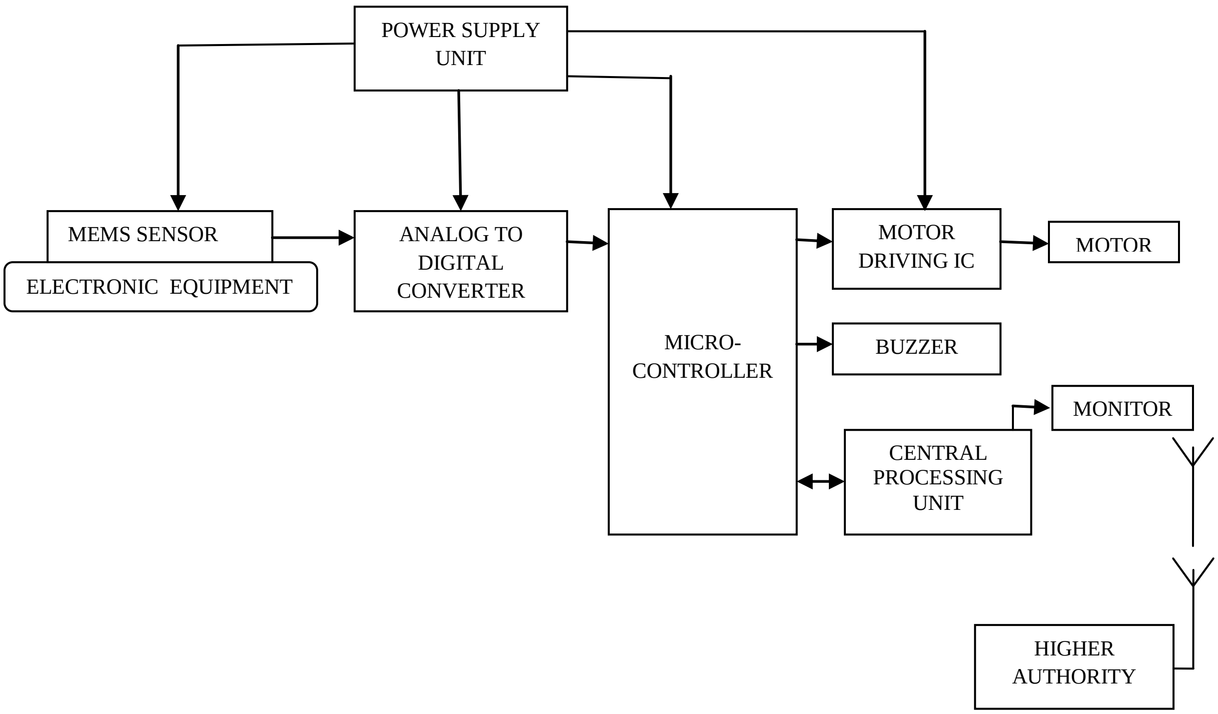


Fig 1: Functional Block Diagram of the System

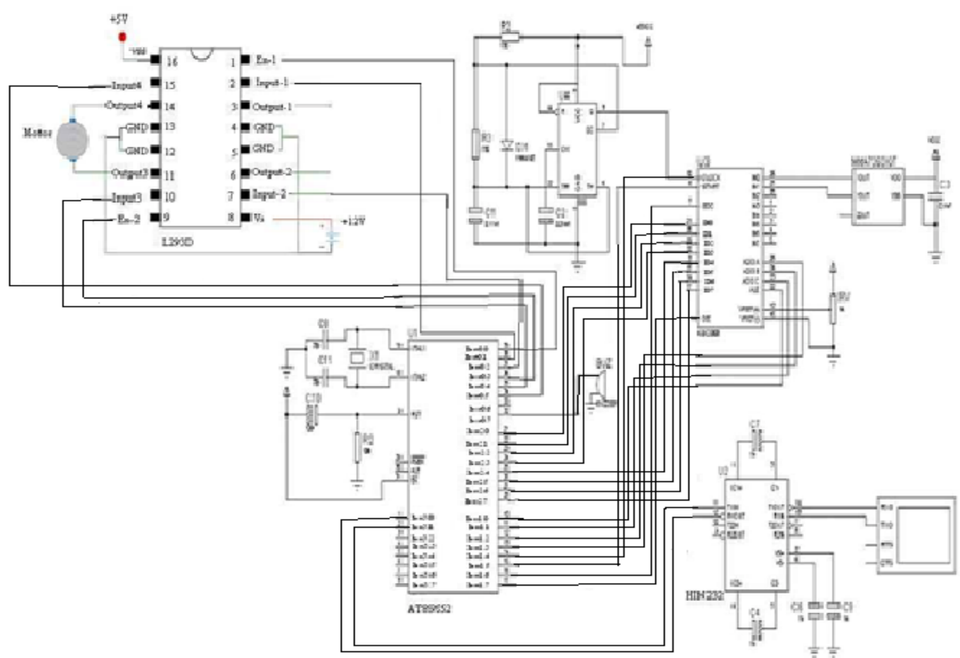


Fig 2: Functional Circuit Diagram of the System

4.EXPLANATION

MEMS is used to detect the unwanted vibrations in the securable equipment and provides the corresponding output signal.Electronic equipment is an electronic device or equipment for which security has to be maintained to protect it from thefts.Power Supply unit is used to supply the electrical power to all the units in the system. The output of a MEMS sensor is an analog signal.To interface this analog signal with a micro controller, first it is converted into a digital signal. So an Analog to Digital converter is used to interface the output of MEMS sensor with the micro controller.

The ATMEL AT89S52 microcontroller is used in implementing the system.For closing the doors of the security room containing the equipment motor and its driving IC is used. A magnetic buzzer is used to produce alarm sounds to alert the security, when the theft is detected.

The Micro Controller is interfaced with a Personal Computer, in order to observe the graphical display of vibrations in the securable equipment. Monitor displays the variations in the vibrations of our securable equipment in the graphical form. GSM stands for Global System for Mobile Communication. It is used to send the alert message to the higher authorities mobile phones.

4.1 MEMS MMA7260QT

The MMA7260QT low cost capacitive micro machined accelerometer features signal conditioning, a 1-pole low pass filter, temperature compensation and g-Select which allows for the selection among 4 sensitivities. Zero-g offset full scale span and filter cut-off are factory set and require no external devices. Includes a Sleep Mode that makes it ideal for handheld battery powered electronics.

FUNCTIONAL BLOCK- DIAGRAM OF MMA7260QT

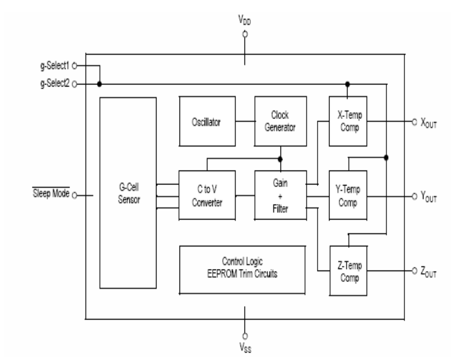


Fig 3: Functional Block Diagram of MMA7260QT

PIN CONFIGURATION

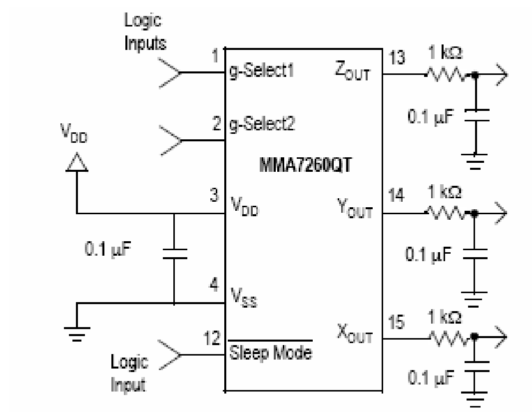


Fig 4: Accelerometer with recommended connection diagram

PIN DESCRIPTION

Pin No.	Pin Name	Description
1	g-Select1	Logic input pin to select g level.
2	g-Select2	Logic input pin to select g level.
3	V_{DD}	Power Supply Input
4	V_{SS}	Power Supply Ground
5 - 7	N/C	No internal connection. Leave unconnected.
8 - 11	N/C	Unused for factory trim. Leave unconnected.
12	Sleep Mode	Logic input pin to enable product or Sleep Mode.
13	Z_{OUT}	Z direction output voltage.
14	Y_{OUT}	Y direction output voltage.
15	X_{OUT}	X direction output voltage.
16	N/C	No internal connection. Leave unconnected.

5. OPERATING PRINCIPLE

The Free scale accelerometer is a surface-micro machined integrated-circuit accelerometer. The device consists of two surface micro machined capacitive sensing cells (g-cell) and a signal conditioning ASIC contained in a single integrated circuit package.The Sensing elements are sealed hermetically at the wafer level using a bulk micro machined cap wafer.

The g-cell is a mechanical structure formed from semiconductor materials (polysilicon) using semiconductor processes (masking and etching). It can be modeled as a set of beams attached to a movable central mass that move between fixed beams. The movable beams can be deflected from their rest position by subjecting the system to an acceleration.

As the beams attached to the central mass move, the distance from them to the fixed beams on one side will increase by the same amount that the distance to the fixed beams on the other side decreases. The change in distance is a measure of acceleration. The g-cell beams form two back-to-back capacitors.

As the center beam moves with acceleration, the distance between the beams changes and each capacitor's value will change, ($C = A\varepsilon/D$). Where A is the area of the beam, ε is the dielectric constant, and D is the distance between the beams.

The ASIC uses switched capacitor techniques to measure the g-cell capacitors and extract the acceleration data from the difference between the two capacitors. The ASIC also signal conditions and filters (switched capacitor) the signal, providing a high level output voltage that is ratio metric and proportional to acceleration.

ADC0808

The ADC0808 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and successive Approximation registers. The 8-channel multiplexer can directly access any of 8-single-ended analog signals. The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors and microcontrollers is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE outputs.

The design of the ADC0808 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications.

INTERNAL BLOCK DIAGRAM

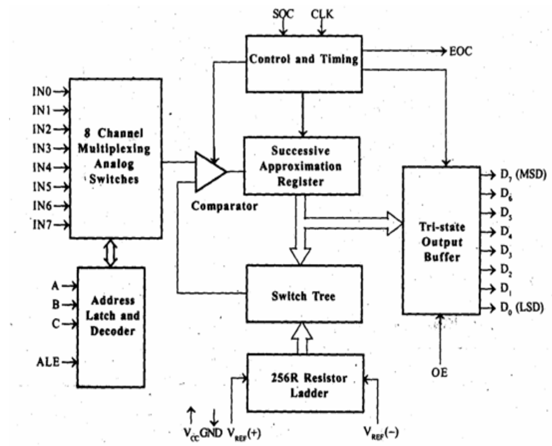


Fig 5: Internal Block Diagram

The various functional blocks of ADC are 8-channel multiplexer, comparator, 256R resistor ladder, switch tree, successive approximation register, output buffer, address latch and decoder.

The 8-channel multiplexer can accept eight analog inputs in the range of 0 to 5V and allow one by one for conversion depending on the 3-bit address input giving to the Address latch and decoder block. The channel selection logic is as shown in below table.

Address Input			Selected Channel
C	B	A	
0	0	0	IN0
0	0	1	IN1
0	1	0	IN2
0	1	1	IN3
1	0	0	IN4
1	0	1	IN5
1	1	0	IN6
1	1	1	IN7

The successive approximation register (SAR) performs eight iterations to determine the digital code for input value.

The SAR is reset on the positive edge of START pulse and start the conversion process on the falling edge of START pulse.

A conversion process will be interrupted on receipt of new START pulse.

The End-Of-Conversion (EOC) will go low between 0 and 8 clock pulses after the positive edge of START pulse.

The ADC can be used in continuous conversion mode by tying the EOC output to START input. In this mode an external START pulse should be applied whenever power is switched ON.

The 256R resistor network and the switch tree is shown in figure 6

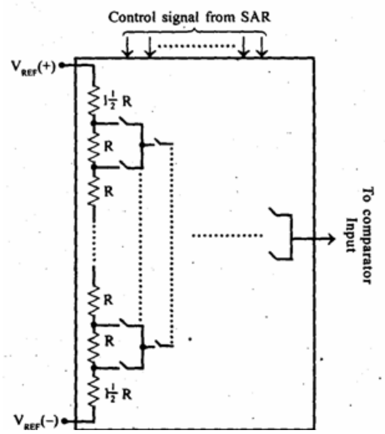


Fig 6: 256R Resistor Ladder Network

The 256R ladder network has been provided instead of conventional R/2R ladder because of its inherent monotonic, which guarantees no missing digital codes.

Also the 256R resistor network does not cause load variations on the reference voltage. The comparator in ADC0808 is a chopper- stabilized comparator. It converts the DC input signal into an AC signal, and amplifies the AC sign using high gain AC amplifier. Then it converts AC signal to DC signal. This technique limits the drift component of the amplifier, because the drift is a DC component and it is not amplified/passed by the AC amplifier. This makes the ADC extremely insensitive to temperature, long term drift and input offset errors.

In ADC conversion process the input analog value is quantized and each quantized analog value will have a unique binary equivalent.

5.1 555 TIMER IC

The NE555 IC monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA.

5.1.1 OPERATION

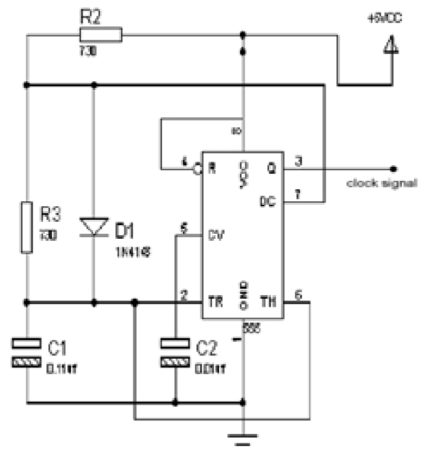


Fig 7: Circuit diagram of IC 555 timer operating as Astable multivibrator

The 555 IC is connected as shown in an astable multivibrator. Both the trigger and threshold inputs (pins 2 and 6) to the two comparators are connected together and to the external capacitor. The capacitor charges toward the supply voltage through the two resistors, R1 and R2. The discharge pin (7) connected to the internal transistor is connected to the junction of those two resistors.

When power is first applied to the circuit, the capacitor will be uncharged, therefore, both the trigger and threshold inputs will be near zero volts. The lower comparator sets the control flip-flop causing the output to switch high. That also turns off transistor T1. That allows the capacitor to begin charging through R1 and R2. As soon as the charge on the capacitor reaches 2/3 of the supply voltage, the upper comparator will trigger causing the flip-flop to reset. That causes the output to switch low. Transistor T1 also conducts. The effect of T1 conducting causes resistor R2 to be connected across the external capacitor. Resistor R2 is effectively connected to ground through internal transistor T1. The result of that is that the capacitor now begins to discharge through R2.

As soon as the voltage across the capacitor reaches 1/3 of the supply voltage, the lower comparator is triggered. That again causes the control flip-flop to set and the output to go high. Transistor T1 cuts off and again the capacitor begins to charge. That cycle continues to repeat with the capacitor alternately charging and discharging, as the comparators cause the flip-flop to be repeatedly set and reset. The resulting output is a continuous stream of rectangular pulses.

The frequency of operation of the astable circuit is dependent upon the values of R1, R2, and C. The frequency can be calculated with the formula f=1/(.693 x C x (R1 + 2 x R2)).

The Frequency f is in Hz, R1 and R2 are in ohms, and C is in farads.

The time duration between pulses is known as the 'period', and usually designated with a 't'. The pulse is on for t1 seconds, then off for t2 seconds. The total period(t) is t1+t2.That time interval is related to the frequency by the familiar relationship

$$f = 1/t \quad \text{or} \quad t = 1/f$$

The time intervals for the on and off portions of the ouput depend upon the values of R1 and R2. The ratio of the time duration when the ouput pulse is high to the total period is known as the duty-cycle. The duty-cycle can be calculated with the formula

$$D = t1/t = (R1 + R2) / (R1 + 2R2)$$

Calculate t1 and t2 times with the formulas below

$$t1 = 0.693(R1+R2)C$$
$$t2 = 0.693 \times R2 \times C$$

The 555 IC in Astable mode of operation, can produce duty-cycles in the range of approximately 55 to 95%. A duty-cycle of 80% means that the ouput pulse is on or high for 80% of the total period. The duty-cycle can be adjusted by varying the values of R1 and R2.

5.2 MOTOR DRIVING IC L293D

In order to drive the motor we need motor drives. Here motor drive used is IC L293D.This IC helps to interface motor to circuit.

PIN CONFIGURATION

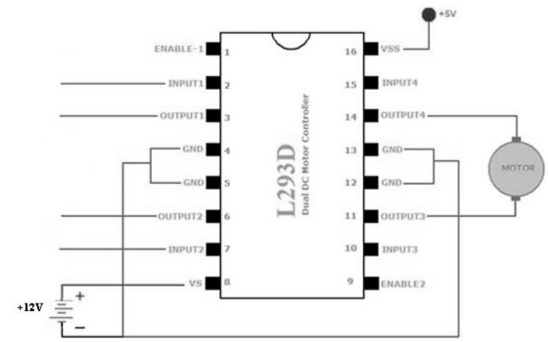


Fig 8 : Pin diagram of IC L293D

The L293D is a quadruple high-current half-H driver IC. The L293D is designed to provide bidirectional drive currents of up to 600-mA at voltages from 4.5 V to 36 V. It is designed to drive inductive loads such as relays, solenoids, dc and bipolar stepping motors, as well as other high-current/high-voltage loads in positive-supply applications .All inputs are TTL compatible.

Each output is a complete totem-pole drive circuit, with a darling ton transistor sink and a pseudo-Darlington source. Drivers are enabled in pairs, with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high , the associated drivers are enabled, and their outputs are active and in phase with their inputs. When the enable input is low, those drivers are disabled, and their outputs are off and in the high-impedance state. With the proper data inputs, each pair of drivers forms a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

5.2.1 LOGIC DIAGRAM

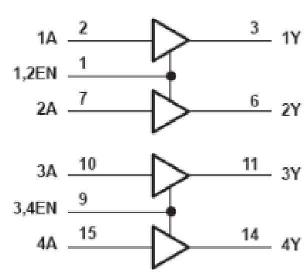


Fig 9 : Logic diagram of IC L293D

FUNCTIONAL TABLE

INPUTS		OUTPUTS
A	EN	
H	H	H
H	L	L
X	L	Z

Where H = high level,
L = low level,
X = irrelevant,
Z=high impedance (off)

In the thermal shutdown mode, the output is in the high-impedance state, regardless of the input levels.

5.2.2 TMB12C2305PX BUZZER

Buzzers like the TMB-series are magnetic audible signal devices with built-in oscillating circuits. The construction combines an oscillation circuit unit with a detection coil, a drive coil and a magnetic transducer. Transistors, resistors, diodes and other small devices act as circuit devices for driving sound generators. With the application of voltage, current flows to the drive coil on primary side and to the detection coil on the secondary side. The amplification circuit, including the transistor and the feedback circuit, causes vibration. The oscillation current excites the coil and the unit generates an AC magnetic field corresponding to an oscillation frequency. This AC magnetic field magnetizes the yoke comprising the magnetic circuit. The oscillation from the intermittent magnetization prompts the vibration diaphragm to vibrate up and down, generating buzzer sounds through the resonator.

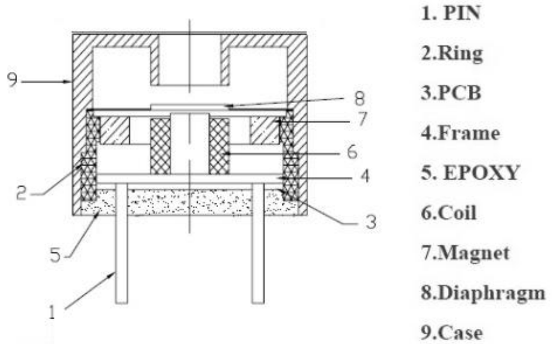


Fig 10 : Internal Structure of Magnetic Buzzer

Here we use a magnetic buzzer in order to generate a buzzer sound at the time of theft , to alert the security by using MEMS sensor based security system.

HIN232

The HIN232 families of RS232 transmitters/receivers interface circuit meets all EIA RS-232 and V.28 specifications, and are particularly suited for those applications where ±12V is not available. They require a single +5v power supply and feature onboard charge pump voltage converters which generate +10V and- 10V supplies from the 5V supply.

The family of devices offers a wide variety of RS232 transmitters/receivers combinations to accommodate various applications. The drivers feature true TTL/CMOS input compatibility. Slew rate limited output, and 300ohms power-off source impedance. The receivers can handle up to ±30V, and have 3k to 7k ohms input impedance.

RS-232 stands for Recommend Standard number 232 and C is the latest revision of the standard. The serial ports on most computers use a subset of the RS-232C standard. The full RS-232C standard specifies a 25-pin "D" connector of which 22 pins are used. Most of these pins are not needed for normal PC communications, and indeed, most new PCs are equipped with male D type connectors having only 9 pins.

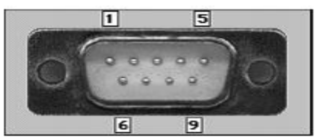


Fig 11 : RS 232 cable

5.3 POWER SUPPLY

The power supply section is used for generating a constant 5V DC from the 230V AC mains power supply.

A step down transformer is used to convert the high voltage AC to a much lesser AC voltage of approximately 12V. A center tapped transformer is used for the step down purpose. The low voltage AC then has to be rectified. For this a full wave rectifier constructed with two diodes is used. The diode used for the rectifier is 1N4007, which is a very easily available diode used for rectifiers.

The rectified voltage is a DC voltage but it is not a constant and smooth DC. Hence a capacitor is used to convert the voltage to a constant and smooth DC voltage. After the filter the voltage is a constant DC but the voltage is much higher than that required by the project. The project requires 5V for the operation of the microcontroller and the other circuits. Hence a LM7805 voltage regulator is used to convert the voltage from the filter to a constant 5V DC. Thus the power from the 230V AC mains is converted into a constant 5V DC for the operation of the circuit.

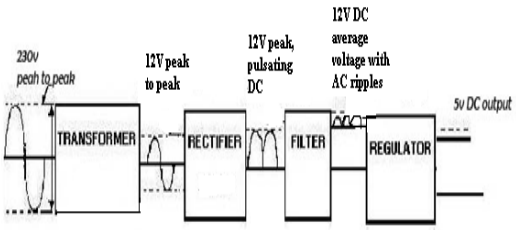


Fig 12 : Signal flow in Power Supply Unit

6. ARCHITECTURE OF THE GSM NETWORK

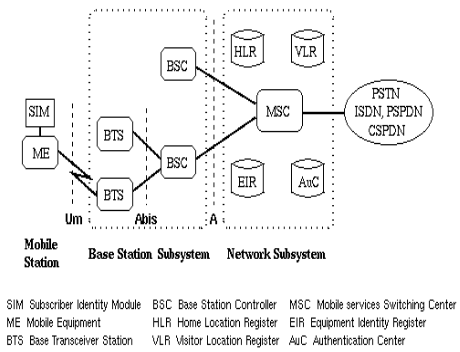
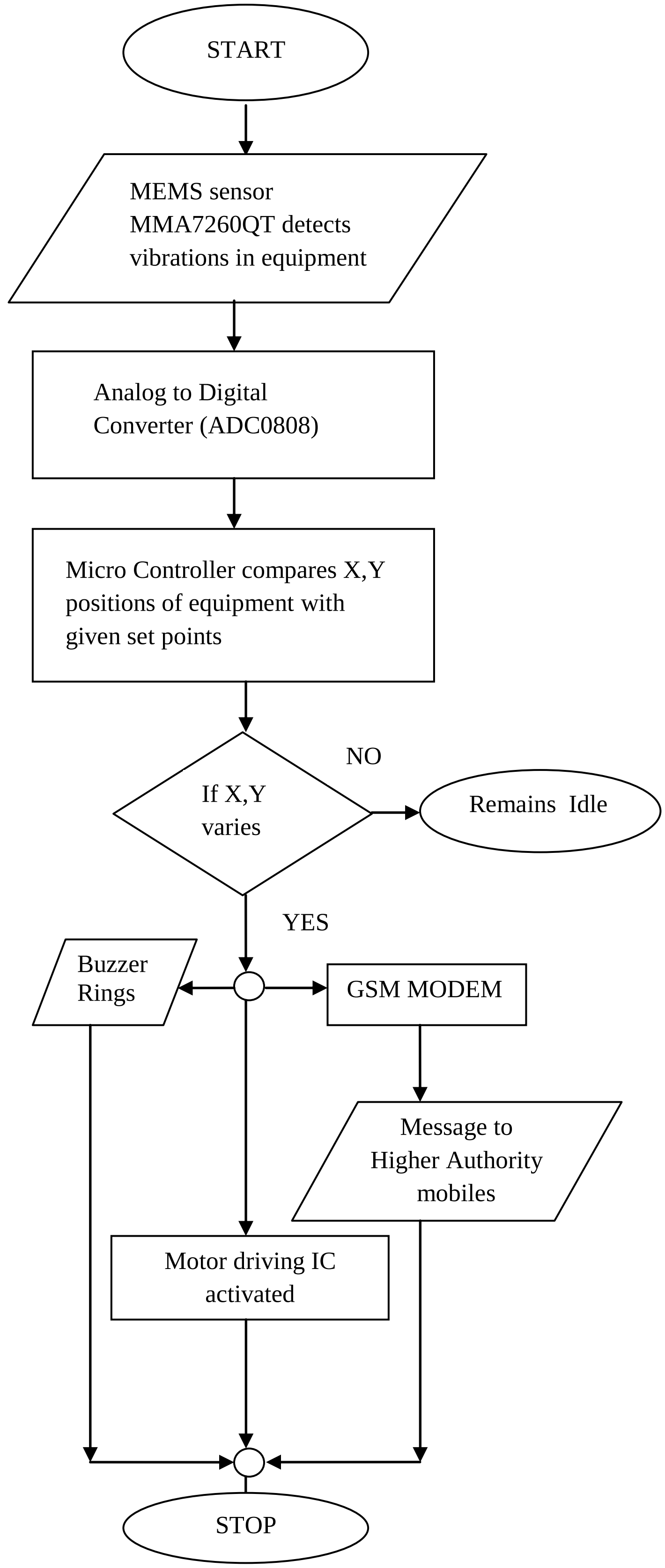


Fig 13 : Architecture of a general GSM network

A GSM network is composed of several functional entities, whose functions and interfaces are specified. Figure 13 shows the layout of a generic GSM network. The GSM network can be divided into three broad parts. The Mobile Station is carried by the subscriber. The Base Station Subsystem controls the radio link with the Mobile Station. The Network Subsystem, the main part of which is the Mobile services Switching Center (MSC), performs the switching of calls between the mobile users, and between mobile and fixed network users. The MSC also handles the mobility management operations. Not shown is the Operations and Maintenance Center, which oversees the proper operation and setup of the network. The Mobile Station and the Base Station Subsystem communicate across the Um interface, also known as the air interface or radio link. The Base Station Subsystem communicates with the Mobile services Switching Center across the A interface.

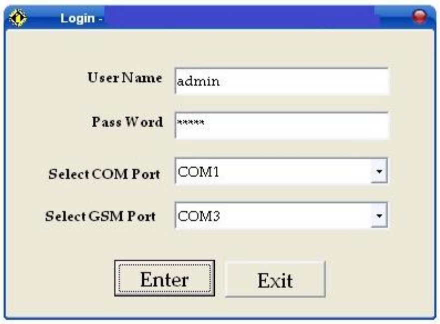
6.1 FLOW CHART

The flow chart for implementing the system is as shown.

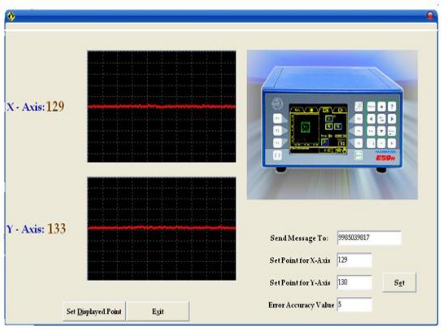


7. EXPERIMENTAL RESULTS & CONCLUSIONS

The following screens are developed using Visual Basic Software login,for providingsetpoints and to display security alert.



LOGIN SCREEN



NORMAL SCREEN

SECURITY ALERT SCREEN

MEMS are going to be the future of the modern technical field in the growth of micro sensor based applications such as automotive industries, wireless communication, security systems, bio medical instrumentation and in armed forces.

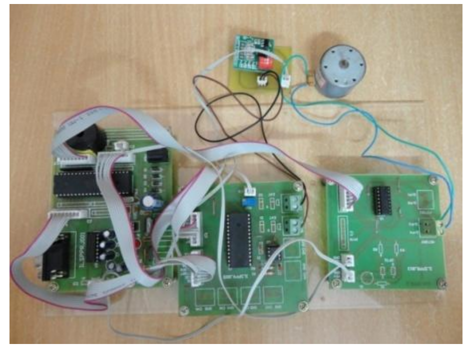


Fig 13 : Hardware Unit

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