Design of 1-bit Full Adder/ Subtractor Circuit using a new 5x5 Fault Tolerant Reversible Gate for Multiple Faults Detection and Correction

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***Abstract*: In future Reversible logic is a prominent technology, having its applications in diverse fields such as low power CMOS, nano-computing and optical computing. In Reversible logic circuits for every distinct input combination an unique output can be produced and vice-versa. In reversible circuits there is one-to-one mapping between input and output vectors. In this paper a New 5X5 Fault Tolerant Reversible Gate (FTRG) is proposed. The proposed gate is universal gate that it can be used to synthesize any arbitrary Boolean function. The proposed gate preserves parity suitable to detect and correct odd number of faults present in the circuit. With a single FTRG gate 1-bit Full Adder / Subtractor circuit can be realized. This proposed gate can be used as a basic building block in designing arithmetic and logic circuits**

***Keywords*:** Adder, Fault tolerance, Garbage output, Parity, Reversible logic, Reversible gate, Subtractor**.**

I. Introduction

Ultra low power dissipation is the quench of today's computing world. Advancement in technology has given scope to design complex systems with higher clock frequency and increase in more packing transistors which results in more power dissipation. In conventional computer all logical operations are irreversible. That is, whenever a logical operation is performed information about the input is erased or lost and is dissipated in the form of heat. Landauer [1] has proven that kTln2 joules of heat energy would be dissipated for each bit of information lost, where k is Boltzmann's constant and T the absolute temperature at which computation is performed.

Bennett[2] proved that kTln2 energy dissipation would not occur, when computation is performed in reversible way. The energy dissipation in a system is having direct relationship with the number of bits erased during computation. Bennett's theorem about heat dissipation is only a necessary condition but not sufficient, but in future technology reversible gates should be used to reduce power dissipation. According to Moore's law for every 18 months the number of transistors packed on chip is doubled which inturn increases power dissipation. More heat is dissipated in irreversible technologies, which reduces the life of the circuit

II. Reversible Logic

Reversible logic circuits are different from that of traditional irreversible circuits. For every distinct input combination reversible circuits can produce unique output, and vice versa. In the reversible circuits, there is a one-to-one mapping between input and output vectors. Reversible computation can be achieved only when the system comprises of reversible gates. Information is not erased in reversible logic operations which in turn dissipates very less heat.

If a reversible gate has 'k' inputs, and therefore 'k' outputs, then it is a 'k x k' reversible gate. In a reversible circuit, the outputs that are not used as an input to the other gate or as primary outputs are called as garbage outputs. The input lines that are tied to logic low or logic high can be called as constant inputs. An efficient reversible circuit design should have minimum number of garbage outputs and constant inputs.

In open literature many 2x2, 3x3, 4x4 reversible gates and parity preserving gates are reported. Few reversible logic gates are presented below

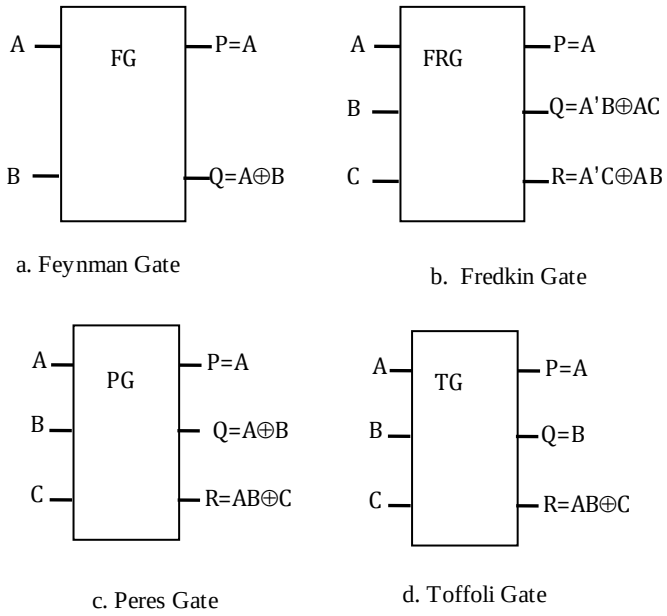

Figure 1. Reversible logic gates

III. Fault Tolerance

Fault tolerance is the property that enables a system to continue operating properly even in the event of the failure of some its components. If the system is designed by using fault tolerant components, then the correction and detection of faults will be possible.

In order to achieve fault tolerance, fault detection and correction should be done. Parity preserving gates are used to detect errors. Many error correction techniques are available.

In this paper redundancy technique is used for error correction.

A gating network is said to be parity preserving when every gate is parity preserving. So, parity preserving reversible circuits require parity preserving reversible logic gates to construct. In order to design efficient fault tolerant systems parity preserving gates are required. A reversible gate is called parity preserving reversible gate if its input parity matches with output parity. The parity of the parity preserving reversible logic gate can be verified by doing the EX-OR of all inputs as well as the EX-OR of all the outputs.

For fault correction, redundancy technique is used. Redundancy is the duplication of critical components of a system to increase the reliability of the system, usually in the case of a backup or fail-safe.

IV. A New 5X5 Fault Tolerant Reversible Gate(FTRG)

A New 5x5 Fault Tolerant reversible Gate, FTRG, is shown in Figure.(2). This gate is not an one-through gate. The truth table of the gate is shown in Table(1). From the truth table it can be observed that every output is having unique input. Input can be recovered from output or output from input. Any arbitrary Boolean function can be implemented by using FTRG, so it is called as universal gate. The proposed gate is parity preserving. This can be verified by comparing the parity of the input to the parity of the output that is A⊕B⊕C⊕D⊕E and P⊕Q⊕R⊕S⊕T.

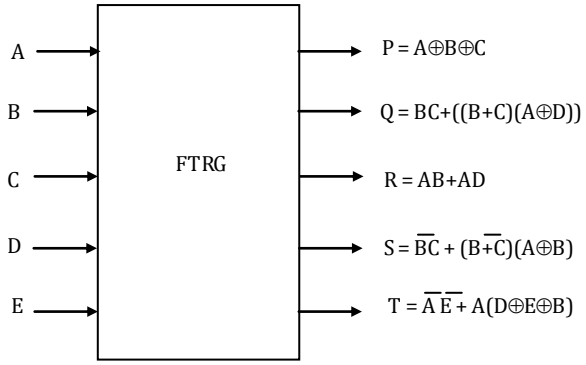

Figure. 2 5X5 Fault Tolerant Reversible Gate

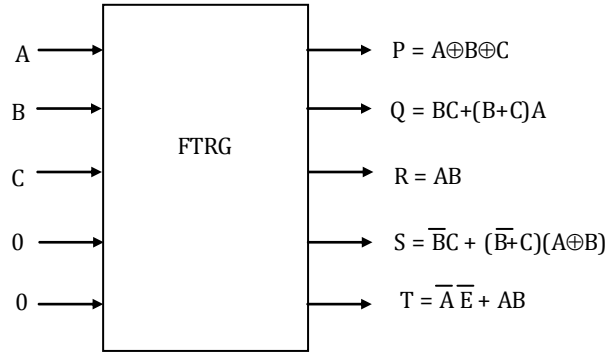

Figure. 3 FTRG as Universal Gate

A	B	C	D	E		P	Q	R	S	T
0	0	0	0	0		0	0	0	1	1
0	0	0	0	1		0	0	0	1	0
0	0	0	1	0		0	0	0	0	1
0	0	0	1	1		0	0	0	0	0
0	0	1	0	0		1	0	0	1	1
0	0	1	0	1		1	0	0	1	0
0	0	1	1	0		1	1	0	1	1
0	0	1	1	1		1	1	0	1	0
0	1	0	0	0		1	0	1	0	1
0	1	0	0	1		1	0	1	0	0
0	1	0	1	0		1	1	1	0	1
0	1	0	1	1		1	1	1	0	0
0	1	1	0	0		0	1	1	1	1
0	1	1	0	1		0	1	1	1	0
0	1	1	1	0		0	1	1	0	1
0	1	1	1	1		0	1	1	0	0
1	0	0	0	0		1	0	0	0	0
1	0	0	0	1		1	0	0	0	1
1	0	0	1	0		1	0	1	1	1
1	0	0	1	1		0	1	0	1	0
1	0	1	0	0		0	1	0	1	1
1	0	1	0	1		0	1	0	1	1
1	0	1	1	0		0	0	1	1	1
1	0	1	1	1		0	0	1	1	0
1	1	0	0	0		0	1	0	0	1
1	1	0	0	1		0	1	0	0	0
1	1	0	1	0		0	0	1	0	0
1	1	0	1	1		0	0	1	0	1
1	1	1	0	0		1	1	0	0	1
1	1	1	0	1		1	1	0	0	0
1	1	1	1	0		1	1	1	1	0
1	1	1	1	1		1	1	1	1	1

Table 1. Truth table of FTRG.

V. Detection and Correction of Faults in Reversible Logic Design

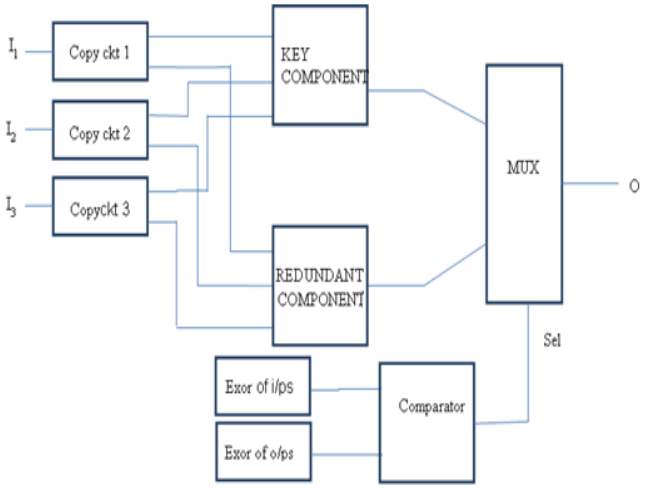

Figure 4. Fault Tolerance design method in Reversible Logic

Figure. 4 shows the implementation of fault tolerance design in reversible logic circuits. Key component preserves the parity to detect the fault. Redundant component is used for correcting the fault. Copy circuits are used because fan out is not allowed in reversible logic. Comparator is used to compare input parity and output of the parity. Output comparator is used as a selection line for multiplexer and which will decide from where to take output.

VI. Fault Tolerant 1-Bit Full Adder/ Subtractor using FTRG

Many implementations of reversible full adder circuits are available in the literature. A reversible full adder circuit will be realized with at least one constant input and two garbage outputs . The above said statement is not valid for fault tolerant reversible full adder circuit. Because in a fault tolerant full adder circuit the parity should be matched on the both sides.To realize a reversible full adder/subtractor with fault tolerance property needs at least three garbage outputs and two constant inputs. In this paper design of reversible full adder with fault tolerance property is implemented with minimum number constant inputs and garbage outputs.

Fault Tolerant Reversible Adder/Subtractor can be achieved through FTRG as shown in Figure. 5 by assigning A, B, and C to the first, second and third inputs of the full adder/subtractor circuit, D is the selection input (If D=0 adder, D=1 Subtractor) and E is the constant input. The ouput P is the sum/difference and the output Q is the carry/borrow, the remaining outputs are the garbage outputs. Truth Table for 1-bit Full adder/ Subtractor is given in Table. 2

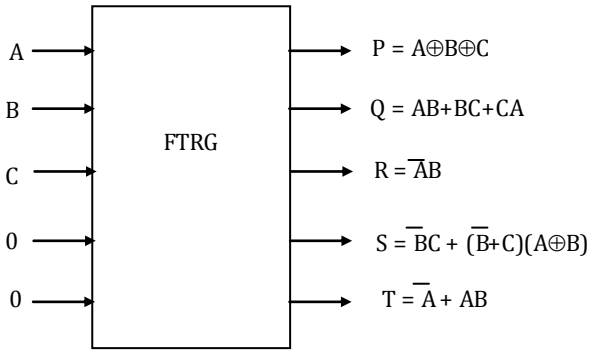

Figure. 5.a FTRG as 1 Bit Full adder

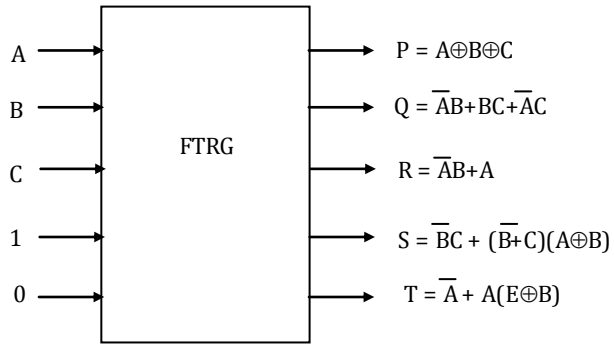

Figure 5.b FTRG as 1 bit full subtractor

Figure. 5 FTRG as full adder / Subtractor

A	B	C	D		S/D	C/B
0	0	0	0		0	0
0	0	0	1		0	0
0	0	1	0		1	0
0	0	1	1		1	1
0	1	0	0		1	0
0	1	0	1		1	1
0	1	1	0		0	1
0	1	1	1		0	1
1	0	0	0		1	0
1	0	0	1		1	0
1	0	1	0		0	1
1	0	1	1		0	0
1	1	0	0		0	1
1	1	0	1		0	0
1	1	1	0		1	1
1	1	1	1		1	1

Table. 2 Truth Table for 1-bit Full Adder/ Subtractor

VII. Implementation of Fault Tolerant 1-bit Adder / Subtractor

Implementation of Fault tolerance for 1-bit full adder/subtractor using FTRG gates is shown in figure.6 This design consists of fifteen Feynman (FG) gates , five Fredkin (FRG) gates and two FTPG gates. Feynman gates and Fredkin gates both are reversible gates, Fredkin gates provides parity preserving and used as multiplexer, Feynman gate is used as coping gate and EX-OR gate for parity checking of inputs and outputs. Inputs are A, B, C, D, E and zero. Check is the comparator output, which is used at Fredkin gate to switch between the two FTRG gates. P,Q,R,S,T are the outputs and the remaining bits are intermediate carriers or garbage outputs.

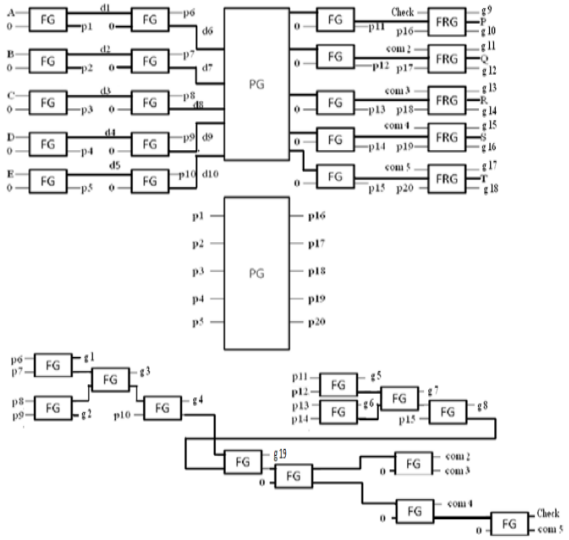

Figure. 6 Implementation of Fault Tolerant Adder/Subtractor using FTRG

*FG =Feynman gate*FRG = Fredkin gate*FTRG = Fault Tolerant Reversible Gate *g = Garbage outputs

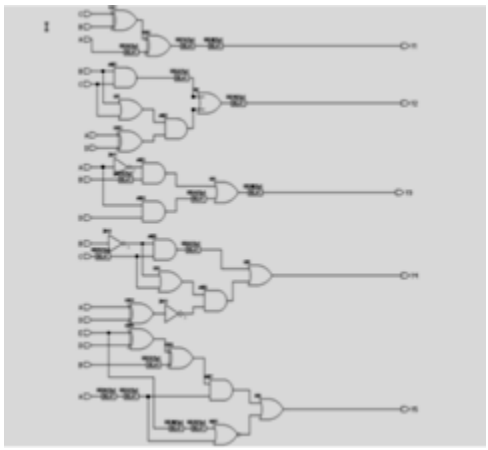

Figure 7. a FTRG gate level design

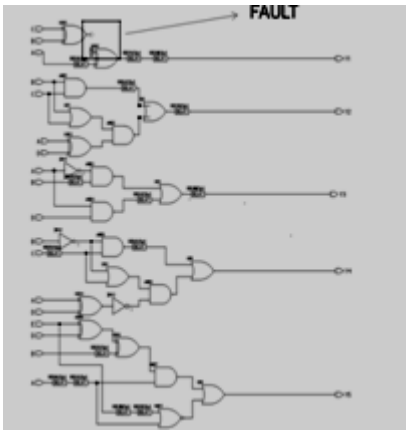

Figure. 7. b Fault in FTRG gate design

Figure. 7 FTRG Gate level Design

Figure(7) shows gate level design and fault in FTRG gate. Fault tolerance of the design is verified by using the fault gate. Faulty gate is obtained by removing the connection at the top of EX-OR gates of FTRG gate.

VIII. Results

The entire architecture was designed using Mentor Graphics tools (Design Architect Tool Kit). The coding is done on Xilinx ISE8.2i on Spartan 3E using target device: 3s500efg320-4 at speed grade of - 4. For simulation purpose the Modelsim6.5se has been used.

Waveforms of FTRG

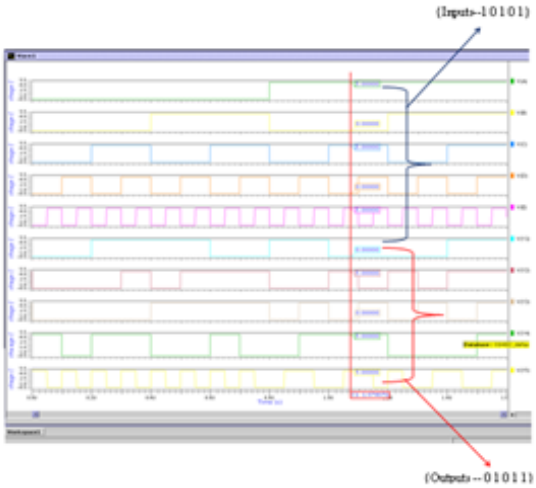

Figure. 8 Waveforms of FTRG as 1-bit Adder/ Subtractor.

Different sets of inputs are given to FTRG gate and the corresponding outputs are shown in Figure.8 When inputs are A=5V, B=0V, C=5V, D=0V, E=5V, outputs are Y_1=0V, Y_2=5V, Y_3= 0V, Y_4=5V, Y_5=5V. It is evident from the results

that FTRG is working as adder when D=0V. and as Subtractor when D=1.

Waveforms of Faulty gate

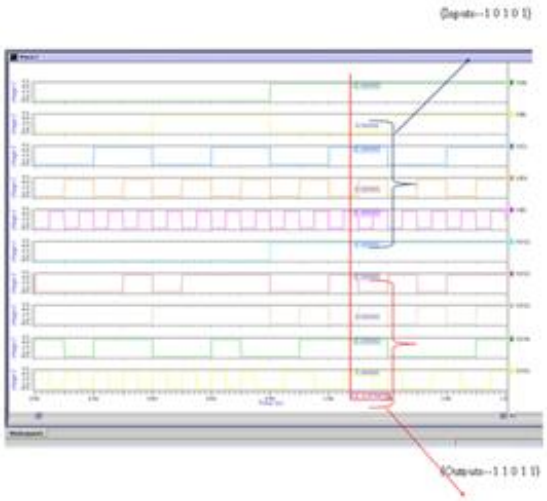

Figure. 9 Waveforms of Faulty gate

From the waveforms of Faulty gate (Figure. 9), when inputs are A=5V, B=0V, C=5V, D=0V, E=5V outputs are Y_1 = 5V, Y_2 = 5V, Y_3= 0V , Y_4=5V and Y_5 = 5V. Fault is introduced in the circuit which leads to Y1=5V instead of 0V as shown in Figure.8. Using this faulty gate single error is created, so there is the mismatch in the parity

Waveforms of 1- bit Fault tolerant Adder/Subtractor

From the waveforms shown in Figure.10 the outputs of Fault tolerant adder/subtractor are Y_1=0V, Y_2=5V, Y_3= 0V , Y_4=5V and Y_5=5V when inputs are A=5V, B=0V, C=5V, D=0V, E=5V. Check signal is 5V which indicates parity mismatch between input and output , in spite of fault it is giving correct results. So fault is tolerated i.e error (odd bit error) detected and corrected.

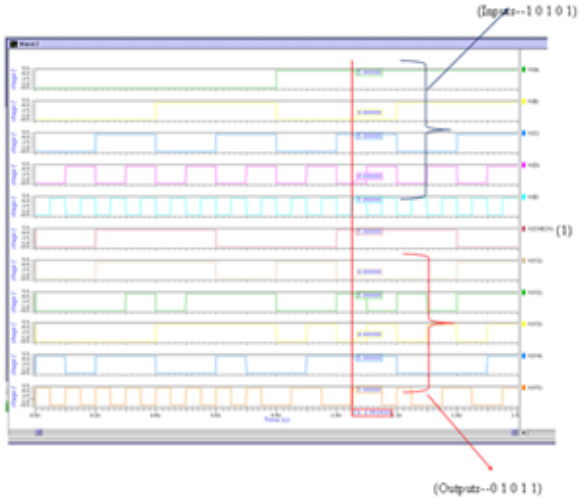

Figure. 10 Waveforms of 1-bit fault tolerant adder / subtractor

IX. Conclusions

From the results presented in Figure. 8 to Figure 10 it is evident that with the proposed 5X5 FTRG the design of 1-bit Fault Tolerant Adder/Subtractor is successfully implemented. The proposed gate is an universal gate which preserves parity and it is suitable to detect and correct odd number of faults present in the circuit. With a single FTRG gate, 1-bit Full Adder/ Subtractor circuit is realized.

This new 5X5 fault tolerant reversible gate can be used as basic building block in designing arithmetic and logic circuits.

References

[1]. Landauer.R, (1961) "Irreversibility and Heat Generation in the Computational Process', IBM Journal of Research and Development, vol 5,pp 183-191.

[2]. Bennett. C.H, (1973) "Logical Reversibility of Computation", IBM J.Research and Development, pp 525-532. [2] Bennett. C.H, (1973) "Logical Reversibility of Computation", IBM J.Research and Development, pp 525-532.

[3]. Islam. M. S, Rahman. M. M, Begum.Z, Hafiz. M. Z and Mahmud. A. A, (2009) "Synthesis of fault tolerant reversible logic circuits", In Proc. IEEE International Conference on Testing and Diagnosis, Chengdu, China, pp 28- 29

[4]. R. Feynman, "Quantum Mechanical Computers," Optics News, Vol. 11, pp. 11–20, 1985.

[5]. E. Fredkin and T. Toffoli, "Conservative logic", Intl. Journal of Theoretical Physics, pp. 219-253, 1982.

[6]. T. Toffoli, "Reversible computing", In Automata, Languages and Programming, Springer-Verlag, pp. 632-644, 1980.

[7]. A. Peres, "Reversible logic and quantum computers", Physical Review: A, vol. 32, no. 6, pp. 3266-3276, 1985. [8] Saiful Islam. Md, Muhammad Mahbubur Rahman, Zerina begum, and Mohd. Zulfiquar Hafiz,(2010) "Efficient Approaches for Designing Fault Tolerant Reversible Carry Look-Ahead and Carry-Skip Adders", The Computing Research Repository (CoRR).

[8]. Saiful Islam. Md, Muhammad Mahbubur Rahman, Zerina begum, and Mohd. Zulfiquar Hafiz,(2010) "Efficient Approaches for Designing Fault Tolerant Reversible Carry Look-Ahead and Carry-Skip Adders", The Computing Research Repository (CoRR).

[9]. Islam. M. S, Rahman. M. M, Begum.Z, Hafiz. M. Z and Mahmud. A. A, (2009) "Synthesis of fault tolerant reversible logic circuits", In Proc. IEEE International Conference on Testing and Diagnosis, Chengdu, China, pp 28- 29.

[10]. Islam. M. S and Begum. Z, (2008) "Reversible logic synthesis of fault tolerant carry skip BCD adder', Bangladesh Academy of Science Journal, vol 32, pp193-200.

[11]. Haghparast. M And Navi. K, (2008) "A Novel Fault Tolerant Reversible Gate for Nanotechnology Based Systems", Am. J. of App. Sci.,vol 5, pp 519-523.

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