MATLAB Simulation of A Interleaved Boost Power factor Correction AC/DC Converter Having Low Switching Losses Used in Plug-in Electric Vehicles

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Abstract

This paper presents a novel, yet simple zero-voltage switching (ZVS) interleaved boost power factor correction (PFC) ac/dc converter used to charge the traction battery of an electric vehicle from the utility mains. The proposed topology consists of a passive auxiliary circuit, placed between two phases of the interleaved front-end boost PFC converter, which provides enough current to charge and discharge the MOSFETs’ output capacitors during turn-ON times. Therefore, the MOSFETs are turned ON at zero voltage. The proposed converter maintains ZVS for the universal input voltage (85 to 265 Vrms), which includes a very wide range of duty ratios (0.07–1). In addition, the control system optimizes the amount of reactive current required to guarantee ZVS during the line cycle for different load conditions. Simulation of both conventional and new IBC is done using MATLAB/SIMULINK and their outputs are compared.

Index Terms: AC/DC converter, continuous current mode (CCM), dc/dc converter, interleaved boost converter, power factor correction (PFC), zero-current switching (ZCS), zero-voltage switching (ZVS).
1. Introduction

Electric vehicle (EV) power conditioning systems usually utilize a high-energy battery pack to store energy for the electric traction system. A typical block diagram of the power conditioning system in an EV is shown in Fig. 1. The high-energy battery pack is typically charged from a utility ac outlet. This energy conversion during the battery charging is performed by an ac/dc converter. Such ac/dc converters, which are used to charge the high-energy battery, usually consist of two stages: front-end boost converter, which performs input PFC and ac/dc conversion, and full-bridge dc/dc converter for battery charging and galvanic isolation. PFC is essential to improve the quality of the input current.

Boost converters are generally used to realize input PFC and ac/dc conversion in the front end of an ac/dc converter. But this method is affecting from high switching loss. The main sources of switching losses in boost PFC converters are hard turn-ON of the MOSFET and the reverse recovery of the boost diode during its turn-OFF.

In order to eliminate the switching losses in a MOSFET-based boost PFC converter, different auxiliary circuits have been used.

Fig. 2. Conventional Interleaved boost PFC schematic

But the key limitations of these type auxiliary circuit for single-switch boost PFC converters are the use of extra semiconductor devices such as diodes and MOSFETs as well as passive components and the extra losses associated with the auxiliary circuit. In resonant-type auxiliary circuits, the main switch can suffer from addition current stress. In this paper, a novel interleaved boost PFC converter is proposed to achieve soft switching in the main switches of the converter. The proposed converter implements soft switching through a simple passive auxiliary circuit placed in between the two phases of the interleaved boost converter. This auxiliary circuit is able to provide reactive current to charge and discharge the output capacitors of the boost MOSFETs and guarantee ZVS.
Since there are no extra semiconductors used in the auxiliary circuit, high efficiency and reliability are the main advantages of the proposed system. Fig.3. shows the power circuit of the ZVS interleaved boost PFC converter.

2. Circuit operations

In this converter, two boost converters operate with 180° phase shift in order to reduce the input current ripple of the converter. This 180° phase shift can be used to provide reactive current for realizing ZVS for power MOSFETs. This auxiliary circuit consists of a HF inductor and a dc-blocking capacitor. Since there may be a slight difference between the duty ratios of the two phases, this dc-blocking capacitor is necessary to eliminate any dc current arising from the mismatch of the duty ratios of the main switches in the practical circuit.

Steady-State Analysis

Mode I (0 < t < t₁) :

This mode starts when the gate pulse is applied to SA1. Once the voltage is applied to the gate, SA1 is turned ON under zero voltage. Since SA1 and SB1 are ON during this interval, the voltage across the auxiliary inductor is zero. Thus, the current through the auxiliary circuit remains constant at I\text{Aux,P}. During this interval, the switch SA1 current, i\text{SA1}, is given by:

\[ I_{SA1}(t) = I_{i} - I_{\text{Aux,P}} - \frac{\text{Vin}}{L_{A}} (t - t_{0}) \]  

(1)

Since the two phases have 180° phase shift, the value of t₁ is given by:

\[ t_{1} - t_{0} = (D - 0.5) T_{s} \]  

(2)

Therefore, the duty ratio is given by:

\[ D = (t_{1} - t_{0}) f_{s} + \frac{1}{2} \]  

(3)

Inserting (2) into (1), the value of the switch current is calculated at t₁

\[ I_{i} = I_{f} - I_{\text{Aux,P}}(t) - \frac{\text{Vin}}{2L_{\text{Aux}}} - \frac{V_{\text{in}}^{2}}{L_{A} f_{s} v_{0}} \]  

(4)

This mode ends once the gate voltage has been removed from SB 1.

Mode II (t₁ < t < t₂) :

This mode is the dead time between the phase B MOSFETs. During this interval, the auxiliary circuit current charges the output capacitance of SB 1 and discharges the output capacitance of SB 2. In this mode, the average voltage across the boost inductance LB is zero. Therefore, the current through LB remains constant at its peak value. The voltage across the auxiliary inductor is given by:

\[ V_{\text{Aux}}(t) = -\frac{V_{0}}{t_{2} - t_{1}} (t - t_{1}) \]  

(5)

Thus, the current through auxiliary circuit is given by:

\[ I_{\text{Aux}}(t) = I_{\text{Aux,P}} - \frac{V_{0}}{2(t_{2} - t_{1}) I_{\text{Aux}}} (t - t_{1})^{2} \]  

(6)

\[ t_{2} - t_{1} = t_{d} \] is the dead time between SB 1 and SB 2. During this period, the output capacitors of the MOSFETs should fully charge and discharge in order to guarantee ZVS for SB 1 and SB 2. Thus, the dead time is calculated as follows
The value of \( L \) in charged. The switch current remains constant.

\[ I_d = \frac{(I_p + I_{AUX,P})L_{AUX}}{V_0} + \sqrt{(I_p + I_{AUX,P})^2 L_{AUX}^2 - 4C_{SOL_{AUX}}} \]

(8)

the current through switch SA1 is calculated as follows,

\[ i_{SA1}(t) = I_V - I_{AUX,P} - \frac{V_m}{L_A} (t-t_0) + \frac{V_0}{2r_d L_{AUX}} (t-t_1)^2 \]

(9)

This mode ends when the output capacitors completely charged and discharged. The switch current \( i_{SA1} \) at this point is given by,

\[ I_2 = I_V - I_{AUX,P} - \frac{V_m}{L_A} (t_d + t_1 - t_0) + \frac{V_0}{2L_{AUX}} t_d \]

(10)

**Mode III (12 < t < 13)**

Once the output capacitors of \( SB \) 1 and \( SB \) 2 have been charged and discharged completely, the gate signal of \( SB \) 2 is applied and \( SB \) 2 is turned ON under ZVS. During this interval, the voltage across the auxiliary circuit is \(-V_0\). The current through the auxiliary inductor, inductor \( LA \) and switch \( SA1 \), is given by

\[ i_{AUX} = I_{AUX,P} - \frac{V_0}{2L_{AUX}} t_d - \frac{V_0}{L_{AUX}} (t-t_2) \]

(11)

\[ i_{LA}(t) = I_V + \frac{V_m}{L_A} (t-t_0) \]

(12)

\[ i_{SA1}(t) = I_V - I_{AUX,P} - \frac{V_m}{L_A} (t-t_0) + \frac{V_0}{2L_{AUX}} t_d - \frac{V_0}{L_{AUX}} (t-t_2) \]

(13)

This mode ends once the gate signal of \( SB \) 2 has become zero \((t_2 = t_0 + 0.5T_s - t_d)\). The value of \( i_{SA1} \) at this point is given by,

\[ I_3(t) = I_V - I_{AUX,P} + \frac{V_m}{2f_s L_A} + \frac{V_0}{2L_{AUX}} t_d + \frac{V_0}{f_s L_{AUX}} (1-D) - \frac{2V_0}{L_{AUX}} t_d \]

(14)

**Mode IV (13 < t < 14)**

During this mode, the output capacitor of \( SB \) 2 is charging from zero to \( V_o \) and the output capacitor of \( SB \) 1 is discharging from \( V_o \) to zero. This period is actually the dead time between \( SB \) 2 and \( SB \) 1 \((t_4 - t_3 = t_d)\). The auxiliary inductor current, the boost inductor current, and the switch current, during this mode, is given by,

\[ I_{AUX}(t) = I_{AUX,P} + \frac{3V_0}{2L_{AUX}} t_d - \frac{V_0}{f_s L_{AUX}} (1-D) \]

\[ - \frac{V_0}{2r_d L_{AUX}} (t-t_3)^2 \]

(15)

\[ I_{LA}(t) = I_V + \frac{V_m}{L_A} (t-t_0) \]

(16)

\[ I_{SA1}(t) = I_V - I_{AUX,P} - \frac{V_m}{L_A} (t-t_0) + \frac{V_0}{2L_{AUX}} t_d - \frac{V_0}{L_{AUX}} (t-t_2) \]

(17)

This mode ends when the gate signal of \( SB \) 1 is applied. The value of \( i_{SA1} \) at this instant is given by

\[ I_4(t) = I_V - I_{AUX,P} + \frac{V_m}{2f_s L_A} + \frac{V_0}{L_{AUX}} t_d + \frac{V_0}{f_s L_{AUX}} (1-D) \]

(18)

**Mode V (14 < t < 15)**

This mode starts when the gate signal is applied to \( SB \) 1. Once the gate has been applied, \( SB \) 1 is turned ON under ZVS. Since \( SA1 \) and \( SB \) 1 are ON during this period, the voltage across the auxiliary inductor is zero; hence, the auxiliary inductor current remains constant at its peak value, \( I_{AUX,P} \). The boost inductor current and the switch current, during this mode, are given by,
\[ I_{LA}(t) = I_v + \frac{V_{in}}{L_A}(t - t_0) \]  
\[ I_{SA1}(t) = I_v - I_{AUX,P} - \frac{V_{in}}{L_A}(t - t_0) \]  
\[ I_{SA1}(t) = I_v + I_{AUX,P} - \frac{V_{in}}{L_A}D \]  
\[ I_{SA2}(t) = I_{AUX,P} + \frac{V_0}{2L_{AUX}}t_d + \frac{V_0}{L_{AUX}}(t - t_6) \]  
\[ I_S(t) = -I_{AUX,P} + \frac{V_0}{2L_{AUX}}t_d + I_p \]  
\[ t_7 = t_6 + \frac{I_{AUX,P} - \left( \frac{V_0}{2L_{AUX}} \right) t_d}{\left( \frac{V_0}{L_{AUX}} \right) + \left( \frac{V_m - V_0}{L_A} \right)} \]  
\[ t_7 = t_6 + \frac{I_{AUX,P} - \left( \frac{V_0}{2L_{AUX}} \right) t_d}{\left( \frac{V_0}{L_{AUX}} \right) + \left( \frac{V_m - V_0}{L_A} \right)} \]  
\[ \text{Mode VIII (t7 < t < t8)}: \]  
\[ \text{During this mode, the output capacitor of } SA1 \text{ is discharging from } V_0 \text{ to zero and the output capacitor of } SA2 \text{ is charging from zero to } V_0. \text{ In this mode, the current through } LA \text{ is at its minimum value } IV \text{ and the excess current from the auxiliary circuit charges and discharges the output capacitors. The auxiliary inductor current is given by:} \]  
\[ i_{AUX}(t) = -I_{AUX,P} + \frac{V_0}{2L_{AUX}}t_d + \]  
\[ \frac{V_0I_{AUX,P} - \left( \frac{V_0}{2L_{AUX}} \right)t_d}{\left( \frac{V_0}{L_{AUX}} \right) + \left( \frac{V_m - V_0}{L_A} \right)} + \frac{V_0}{2L_{AUX}}(t - t_7)^2 \]  
\[ \text{Since this mode is the dead time between } SA1 \text{ and } SA2, \text{ t8 = t7 + td}. \text{ This mode ends once the output capacitors have been charged and discharged.} \]  
\[ \text{Fig. 4 shows the key waveforms of the converter for D>0.5. According to this figure the eight modes of operation is explained above. From Figs. 4, all MOSFETs of the interleaved boost converter are turned ON under zero voltage and the output MOSFETs are turned OFF at nearly zero current. This implies that the MOSFETs enjoy having near-zero switching losses. In order to guarantee ZVS for the MOSFETs, the inductive current of the auxiliary circuit should be enough to neutralize the input current and discharge and charge the output capacitors of the MOSFETs during turn-ON times of } SA1 \text{ and } SB 1. \text{ Also, the dead time between the gate pulses should be enough to allow complete charging and discharging of the output capacitors of the switches} \]
Fig. 4. Key waveforms of the converter for \( D > 0.5 \).

### 3. DESIGN

#### Auxiliary Inductor Design

The auxiliary inductor should be designed so as to provide enough energy to neutralize the energy in the boost inductor as well as charge and discharge the output capacitors of the MOSFETs. Thus, the key design criteria which needs are as follows:

1. Design the auxiliary inductor to have enough energy to be able to neutralize the valley current of the boost inductor and charge and discharge the output capacitors of the MOSFETs.
2. Choose dead time so as to have enough time to completely charge and discharge the output capacitors.

The energy required to neutralize the boost inductor and charge and discharge the output capacitors of the MOSFETs is given by:

\[
W = \frac{1}{2} L_{A} A \left( \frac{P_{in}}{V_{in}} - \frac{V_{in}(1 - \frac{V_{in}}{V_{0}})}{2 I_{A}(f)} \right)^{2} + C_{s0} V_{0}^{2}
\]

(29)

The energy of the auxiliary inductor should be greater or equal to the energy derived in (32). Therefore, we have:

\[
\frac{1}{2} L_{AUX} I_{Aux,p}^{2} \geq \frac{1}{2} L_{A} A \left( \frac{P_{in}}{V_{in}} - \frac{V_{in}(1 - \frac{V_{in}}{V_{0}})}{2 I_{A}(f)} \right)^{2} + C_{s0} V_{0}^{2}
\]

(30)

The peak value of the auxiliary circuit is given by:

\[
I_{Aux,p} = \frac{V_{0}(1 - \frac{V_{in}}{V_{0}})}{2L_{Aux} f}
\]

(31)

Insert in the equation (34) into (33) is given by:

\[
L_{AUX} \leq \frac{V_{in}^{2} \left( \left( \frac{V_{in}}{V_{0}} \right)^{2} \right)^{2} 4 f_{s}^{2}}{A \left( \frac{P_{in}}{V_{in}} - \left( \frac{V_{in}}{V_{0}} \right) \right)^{2} + C_{s0} V_{0}^{2}}
\]

(32)

The dead time can be calculated by using the equation:

\[
I_{d} = \frac{(I_{p} + I_{Aux,p}) L_{Aux}}{V_{0}}
\]

(33)

Therefore, the design procedure is summarized in the following steps.

1. Select the minimum switching frequency, which corresponds to the peak value of the input current.
2. Calculate the value of the auxiliary inductance using (32).
3. Choose dead time so as to have enough time to completely charge and discharge the output capacitors of the MOSFETs using (33).

### 4. CLOSED LOOP CONTROL OF THE CONVERTER
Fig. 5 shows the block diagram of the control system.

The difference between a reference voltage and output voltage given to a voltage controller. That results a current reference, this current reference and magnitude of rectifier output current is added. Then it gives to a current controller. Converter switching frequency compared with output of current controller gives switching pulses. By applying suitable deadtime switching pulses applied to switches. The required auxiliary circuit current for different loads is determined by,

\[ I_{Aux,p} = I_{ref} - \frac{\Delta i_{LA}}{2} + \frac{2C_{s0}v_0}{t_d} \]  \hspace{1cm} (34)

The auxiliary circuit current is given by,

\[ I_{Aux,p} = \frac{v_{in}}{2L_{Aux}f_s} \] \hspace{1cm} (35)

The boost inductor ripple is given by,

\[ \Delta i_{LA} = \frac{v_{in}(1 - \frac{v_{in}}{v_0})}{L_Af_s} \]  \hspace{1cm} (36)

Inserting (36) and (35) into (34) determines the desired switching frequency of the converter

\[ f_{sw} = \frac{v_{in}L_A + v_{in}(1 - \frac{v_{in}}{v_0})L_{aux}}{I_{ref} + \frac{2C_{s0}v_0}{t_d}} \] \hspace{1cm} (37)

5. MATLAB SIMULATIONS
Simulation analysis of both the conventional and the proposed model is done using MATLAB/SIMULINK. The proposed and conventional IBCs are realized using the following table.

<table>
<thead>
<tr>
<th>Parameter’s name</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>( V_{in} )</td>
<td>170V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>( V_o )</td>
<td>430 V</td>
</tr>
<tr>
<td>Inductor</td>
<td>( L_1, L_2, L_{aux} )</td>
<td>4.6mH, 1 20( \mu )H</td>
</tr>
<tr>
<td>Capacitors</td>
<td>( C_{aux} )</td>
<td>1( \mu )F</td>
</tr>
<tr>
<td>Nominal switching frequency</td>
<td>( F_s )</td>
<td>220KHz</td>
</tr>
</tbody>
</table>

Table 1. Circuit parameters

Fig. 6 simulink model of conventional ac/dc boost converter topology
Simulation of both conventional and new IBC has been done with the same input and load conditions in both open loop and closed loop and their outputs are compared.

Fig. 7. The simulink model of Interleaved ZVS ac/dc boost converter with openloop control.
Fig. 8. The complete simulink model of interleaved ZVS ac/dc boost converter with closed loop control.

Fig. 9. Output voltage of a conventional ac/dc boost converter.

Fig. 10. Harmonic content of the current waveform obtained from conventional interleaved PFC. The output voltage of the conventional interleaved ac/dc boost converter shown in the below figure. But the output voltage contains THD=104.89% and power factor is about only .71.

Fig. 11. Output voltage of ac/dc boost converter with open loop control.

Fig. 12. Harmonic content of the current waveform obtained from new interleaved PFC with open loop control. The output voltage of the interleaved ZVS ac/dc boost converter open loop topology is shown in the below figure. By using open loop control the THD is about 58% and power factor is .84.
the THD is approximately 7% and powerfactor is 0.99.

The output voltage of the converter using closed loop control is shown in fig 26. By using closed loop control
6. CONCLUSION

In this paper a soft-switching interleaved boost converter using auxiliary circuit is proposed. Numerical-mode analysis was performed for the design of the proposed ISSBC. The computer simulation of the converter has been carried out using MATLAB. From this analysis, a clear idea regarding the switching is made available. Since the interleaved method distributes the input current according to each phase, it can decrease the current rating of the switching device. Also, it can reduce the input current ripple, output voltage ripple, and size of the passive components. From the analysis of simulation we get 7% of THD in zvs interleaved ac/dc boost converter by using a auxiliary circuit.
REFERENCES


BIOGRAPHIES

Mr. Vinod Soman received the Bachelor's degree in Electrical and Electronics Engg from Government Engg College Idukki, Kerala, India in 2009. He is currently pursuing his M tech degree in Power Electronics & control from Government Engg college Idukki. His current research interests include interleaved ac/dc converters and control systems.