CASCADED MULTILEVEL INVERTER WITH MULTICARRIER PWM TECHNIQUES

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Abstract

Multilevel inverter has so many advantages than conventional two level inverter. As the number of level increases the output approaches to a pure sinusoidal wave.Multilevel inverter using both fundamental frequency switching and higher frequency switching. In this paper discuss only about higher frequency switching.In higher frequency switching we are using two signals, one is reference signal and the other one is carrier signal. For Sinusoidal PWM technique sinusoidal wave be the reference signal and triangular wave be the carrier signal. This paper discuss about SinePWM Techniques with multicarrier. Simulation done on 7 level cascaded H-Bridge inverter with multicarrier SinusoidalPWM technique.

Index Terms:*SinusoidalPWM(SPWM);Alternate Phase Opposite Disposition(APOD);Phase Opposite Disposition(POD);Phase Disposition(PD)*

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1. INTRODUCTION

In recent years, multilevel inverters have received more attention in industrial applications, such as motor drives, staticVAR compensators (STATCOMs)[1],[2], and renewable energy systems. Compared to the traditional two-level voltage source inverters, the stepwise output voltage is the major advantage of multilevel inverters[3]. This advantage results in higher power quality, better electromagnetic compatibility, lower switching losses, higher voltage capability, and needlessness of a transformer at distribution voltage level, thereby reducing the costs. Multilevel inverters are generally divided into three configurations: diode-clamped, flying capacitor, and cascaded H-bridge multilevel inverters.

Regarding the switching frequency of multilevel inverters, the switching strategies can be classified into two categories: strategies that work with high switching frequencies, including the classical carrier-based sinusoidal pulse width modulation (PWM) strategy[4], and those that work with low switching frequencies, generally equal to the fundamental component frequency, and generate a staircase waveform

2. CASCADE H-BRIDGES INVERTER

The cascade H-bridges inverter is a cascade of H-bridges, or H-bridges in a series configuration. In this topology the H-bridges are cascaded in every phase [5]. The output voltage of cascaded multilevel inverter is equal to sum of the output voltages of the individual bridges and can be controlled to produce a staircase waveform. With the increase in H- bridges in a phase, the output voltage waveform tends to be more sinusoidal. Figure 1 shows its 7-level topology. It consists of three identical H-bridges in each phase. In n-level topology, (n-1)/2 identical H- Bridges are used in every phase. There must be a separate DC source for the DC bus of every individual H-bridge. Hence, this topology is useful for collecting energy from renewable energy resources e.g. solar panels and fuel cell.

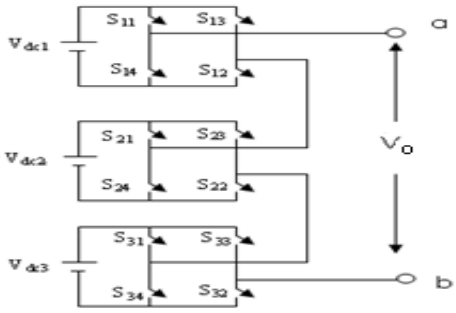

Figure 1: Single Phase 7 level Cascaded H-Bridge inverter

3. MULTI LEVEL INVERTER MODULATION CONTROL SCHEMES

Figure 2 shows the multilevel converter modulation methods. The modulation control schemes for the multilevel inverter can be divided into two categories[6], fundamental switching frequency and high switching frequency PWM such as multilevel carrier-based PWM, selective harmonic elimination and multilevel space vector PWM Multilevel SPWM needs multiple carriers. Each DC source needs its own carrier. Several multi-carrier techniques have been developed to reduce the distortion in multilevel converters, based on the conventional SPWM with triangular carriers. Some methods use carrier disposition and others use phase shifting of multiple carrier signals. By generalizing, for an 'n' level multilevel inverter, (n-1) carriers are needed [7].

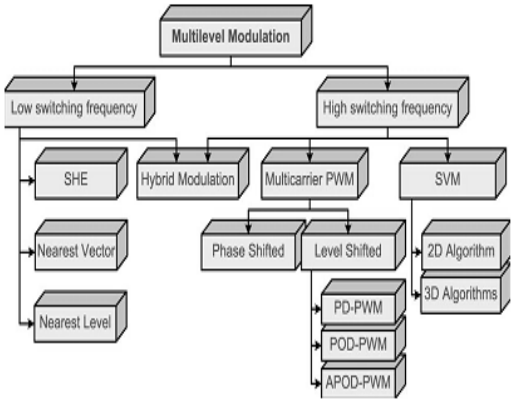

Figure 2: Multilevel converter modulation methods

One of the most straightforward methods of describing voltage-source modulation is to illustrate the intersection of a modulating signal (duty cycle) with triangle waveforms. There are three alternative PWM strategies with differing phase relationships:

- Alternate phase disposition (APOD) – every carrier waveform is in out of phase with its neighbour carrier by 180^0.
- Phase opposition disposition (POD) – All carrier waveforms above zero reference are in phase and are 180^0 out of phase with those below zero.
- Phase disposition (PD)- All carrier waveforms are in phase.

4. ALTERNATE PHASE DISPOSITION (APOD)

In case of alternate phase disposition (APOD) modulation, every carrier waveform is in out of phase with its neighbour carrier by 180^0.

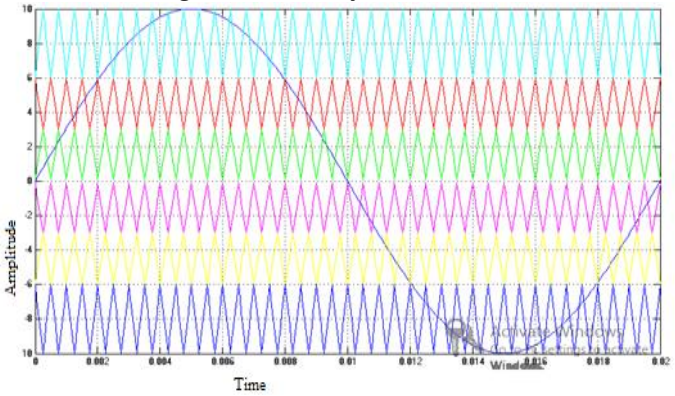

Figure 3: Carrier arrangements for APODPWM strategy

The rules for APOD method, when the number of level N = 7, are

- The N – 1 = 6 carrier waveforms are arranged so that every carrier waveform is in out of phase with its neighbour carrier by 180^0.There are 3 positive carriers whose magnitude is positive and 3 negative carriers whose magnitude is negative.
- The converter switches to + Vdc when the reference is greater than 1st positive carrier waveform.
- The converter switches to +2Vdc when the reference is greater than the 2nd positive carrier waveform.
- The converter switches to +3Vdc when the reference is greater than the uppermost 3rd positive carrier waveform.
- The converter switches to 0 when the reference is lesser than all positive carrier waveforms as well as lesser than negative carrier waveforms.

- The converter switches to - Vdc when the reference is lesser than 1st negative carrier waveform.
- The converter switches to - 2Vdc when the reference is lesser than 2nd negative carrier waveform.
- The converter switches to - 3Vdc when the reference is lesser than 3rd lowermost negative carrier waveform.

5. PHASE OPPOSITION DISPOSITION (POD)

For phase opposition disposition (POD) modulation all carrier waveforms above zero reference are in phase and are 1800 out of phase with those below zero.

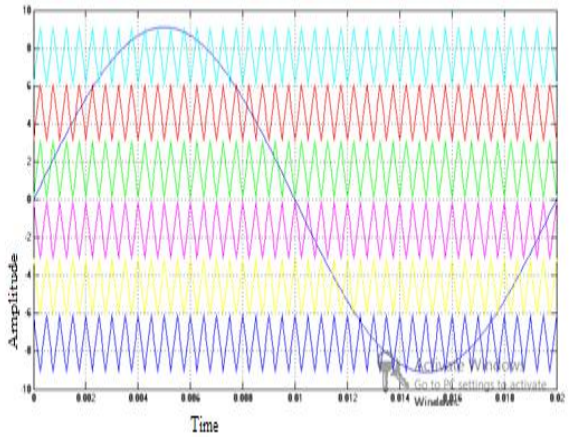

Figure 4: Carrier arrangements for PODPWM strategy

The rules for the phase opposition disposition method, when the number of level N = 7 are

- The N –1 = 6 carrier waveforms are arranged so that all carrier waveforms above zero are in phase and are 180^0 out of phase with those below zero. There are 3 carrier waveforms above the reference zero line and other 3 carrier waveforms with 180^0 degree shift are below the zero reference line.
- The converter switches to + Vdc when the reference is greater than 1st positive carrier waveform.
- The converter switches to +2Vdc when the reference is greater than the 2nd positive carrier waveform.
- The converter switches to +3Vdc when the reference is greater than the uppermost 3rd positive carrier waveform.
- The converter switches to 0 when the reference is lesser than all positive carrier waveforms as well as lesser than negative carrier waveforms.
- The converter switches to - Vdc when the reference is lesser than 1st negative carrier waveform.
- The converter switches to - 2Vdc when the reference is lesser than 2nd negative carrier waveform.
- The converter switches to - 3Vdc when the reference is lesser than 3rd lowermost negative carrier waveform.

6. PHASE DISPOSITION (PD)

For phase disposition (PD) modulation all carrier waveforms above zero reference and below zero reference are in phase.

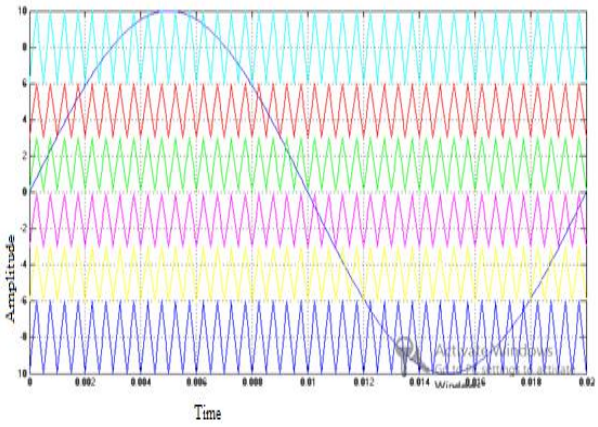

Figure 5: Carrier arrangements for PDPWM strategy

The rules for the phase disposition method, when the number of level N = 7, are

- The N –1 = 6 carrier waveforms are arranged so that all carrier waveforms above zero and below zero are in phase. There are 3 carrier waveforms above the reference zero line and other 3 carrier waveforms below the zero reference line.
- The converter switches to + Vdc when the reference is greater than 1st positive carrier waveform.
- The converter switches to +2Vdc when the reference is greater than the 2nd positive carrier waveform.
- The converter switches to +3Vdc when the reference is greater than the uppermost 3rd positive carrier waveform.
- The converter switches to 0 when the reference is lesser than all positive carrier waveforms as well as lesser than negative carrier waveforms.
- The converter switches to - Vdc when the reference is lesser than 1st negative carrier waveform.

- The converter switches to - 2Vdc when the reference is lesser than 2nd negative carrier waveform.
- The converter switches to - 3Vdc when the reference is lesser than 3rd lowermost negative carrier waveform.

7. SIMULATION RESULTS

The single phase seven level inverter is modelled in SIMULINK using power system block set. The switching pulses for each H-Bridges are generated from different multicarrier sinePWM techniques. From the FFT analysis the % THD value can be calculated.

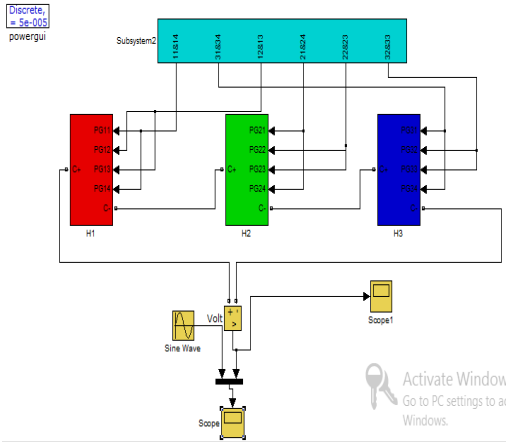

Figure 6: 7 level inverter simulation model

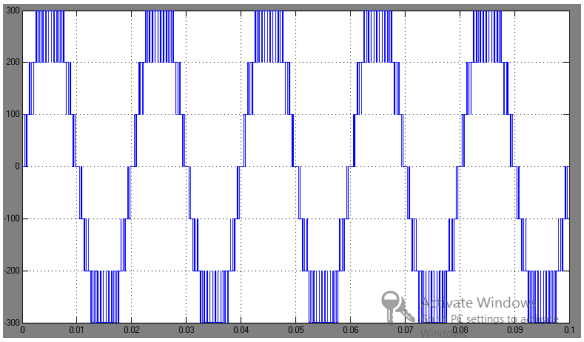

Figure 7: Output voltage generated by APODPWM strategy

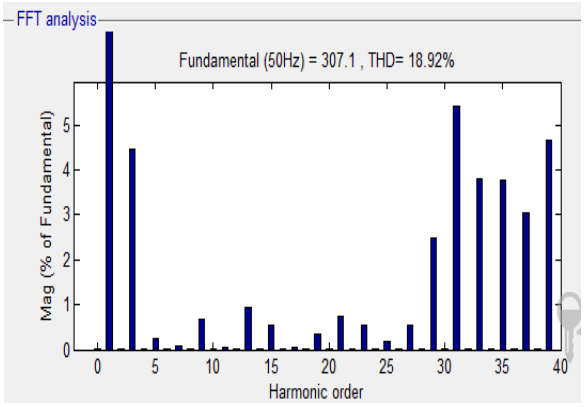

Figure 8: FFT plot for output voltage of APODPWM strategy

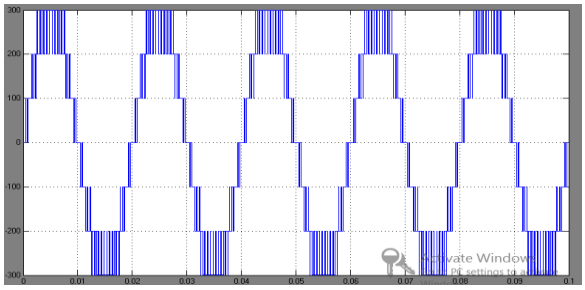

Figure 9: Output voltage generated by APODPWM strategy

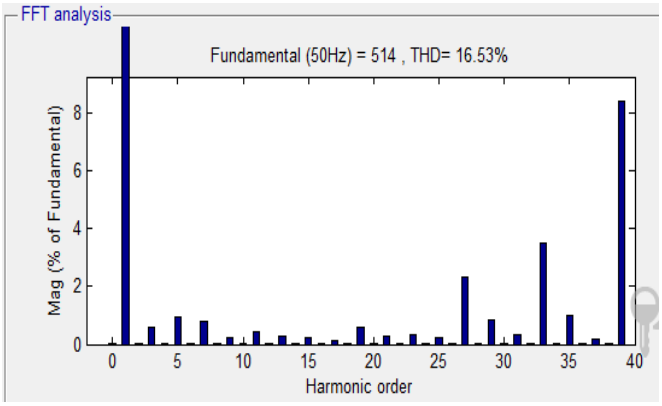

Figure 10: FFT plot for output voltage of PODPWM strategy

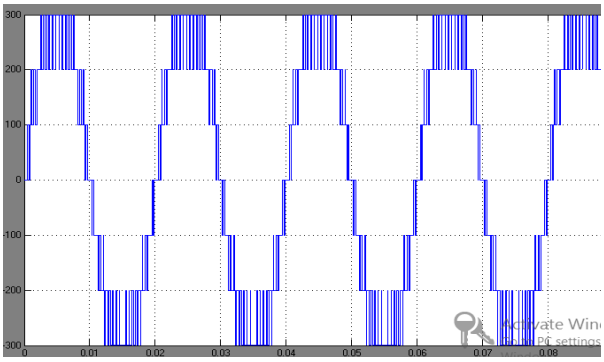

Figure 11: Output voltage generated by PDPWM strategy

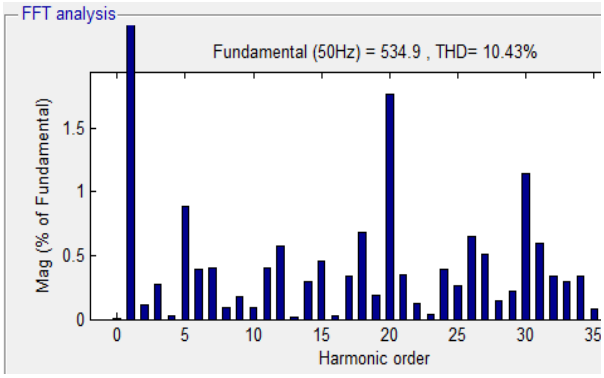

Figure 9: FFT plot for output voltage of PDPWM strategy

8. CONCLUSION

In this paper, multicarrier SinePWM techniques for seven level inverter have been presented. Performance factors like %THD, Vrms, CF and FF have been evaluated presented and analyzed. It is found that the PDPWM and PODPWM strategy provides lower %THD. Depending on the performance measure required in a particular application of chosen MLI based on the output quality appropriate PWM have to be employed.

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