REVIEW ON DESIGN & SIMULATION PARALLEL PIPELINED RADIX -2^2 FFT ARCHITECTURE FOR REAL VALUED SIGNALS

Madhavi S.Kapale[#1],
[1]Student Mtech Electronics Engineering (Communication)
Vidarbha Institute of Technology,Nagpur,India
[1]madhvikapale@gmail.com,

Prof.Nilesh P. Bodne [#2]
[2] Assistant Professor
Vidarbha Institute of Technology,Nagpur , India
[2]nileshbodne@gmail.com

ABSTRACT- ***Fast Fourier transform (FFT) and Inverse Fast Fourier Transform (IFFT) processing is one of the key procedures in popular orthogonal frequency division multiplexing (OFDM) communication systems. Structured pipeline architectures, low power consumption, high speed and reduced chip area are the main concerns in this VLSI implementation. In this paper, the efficient implementation of FFT/IFFT processor for OFDM applications is presented. We adopt single-path delay feedback architecture., this proposed architecture applies a reconfigurable complex multiplier to achieve a reduced ROM size. To reduce the truncation error we adopt the fixed width modified booth multiplier. As a result, the proposed radix-2k feed forward architectures not only offer an attractive solution for current applications, but also open up a new research line on feed forward structures.***

Keywords: Parallel, Radix-2^2 ,FFT, IFFT, OFDM, Modified Booth Multiplier.

1.INTRODUCTION

The Fast Fourier Transform (FFT) is essential in the field of digital signal processing (DSP), widely used in communication systems, especially in orthogonal frequency division multiplexing (OFDM) systems, wireless-LAN, ADSL, VDSL systems and Wi-MAX. Apart from the applications, the system demands high speed of operation, low power consumption, reduced truncation error and reduced chip size. By considering these facts. We proposed the FFT processor with single path delay feedback (SDF) Pipeline architecture with reconfigurable complex constant multiplier and fixed-width modified booth multiplier.

Discrete Fourier transform (DFT) is the useful method to transform from the time domain to the frequency domain. Here 2N2 complex operations are required for the computation of the N-point DFT. There are a number of different 'Fast Fourier Transform' (FFT) algorithms that enable the calculations much faster than a DFT. FFT algorithms used for quick calculation of discrete Fourier transform of a data vector. The FFT is a DFT algorithm which reduces the number of computations needed for *N* points from (*N2*) to (*N* log *N*) where log is the base-2 logarithm. It is the new technique to reduce the order of complexity operations of DFT based on decomposition and breaking the transform into smaller transform and combining them to give the total transform.

FFT is used to speed up the DFT, it reduces the computation time required to compute a discrete Fourier transform and improves the performance by factor 100 or more over direct evaluation of DFT. The SDF pipelined architecture is used for the high-throughput in FFT processor. There are three types of pipeline structures; they are single-path delay feedback (SDF), single-path delay commutator (SDC) and multi-path delay commutator. The advantages of single-path delay feedback (SDF) are (1) This SDF architecture is very simple to implement the different length FFT. (2) The required registers in SDF architecture is less than MDC and SDC architectures. (3) The control unit of SDF architecture is easier. In order to speed up the FFT computation we increase the radix, for reducing the chip size we use ROM-less architecture and for further low power consumption we implement the reconfigurable complex multiplier and delay line buffers[2]-[4], error compensation is carried out using fixed-width modified booth multiplier. Here reconfigurable complex constant multiplier works simultaneously for the multiplication of two pair wise coefficients. These coefficients are real and imaginary with limited number of points and used for the multiplication of twiddle factors in FFT architectures. Several error compensation methods have been used to reduce the truncation error in the multiplication of twiddle factors in

FFT/IFFT processors. Here, this fixed-width modified booth multipliers for loss applications achieve better error performance in terms of absolute error and mean square error. Using radix-4 algorithm, we propose a 64-point FFT/IFFT processor for OFDM applications.

2. LITERATURE REVIEW

"Pipelined Radix-2(k) Feed forward FFT Architectures"[1] this paper extend the use of radix- 2^k to feed forward FFT architectures. It is shown that feed forward structures are more efficient than feed forward structures are more efficient than feedback ones when several samples in parallel must be processed.

"Parallel – Pipelined radix-2^2 fft architecture for real valued signals " [2] This paper has proposed a novel method for the implementation of parallel-pipelined FFT architecture for real –valued signals. It is very suitable for applications in implantable or portable devices because of its low area and power consumption.

"Design of parallel pipelined feed forward architecture for zero frequency & minimum computation algorithm of FFT " [3] This parallel pipelined feed forward architecture paper has presented to design efficient architectures for the computations of RFFT. The computations can be completed by limiting the signal flow graph diagram in to real and imaginary paths this approach is mainly used to effective utilization of memory and to avoid reusability . The approach can be implemented for higher radix algorithms.

"Design of low power, high efficient fft/ifft processor for wireless communication" [4] In this paper, we presented low power high efficient single-path delay feedback pipelined 64-point FFT/IFFT processor for OFDM applications has been described. For improving the speed of the processor we increased the radix size from radix-2 to radix-4. In order reduce the chip size by reducing its area we used the reconfigurable complex constant multiplier which multiplies as well as stores the twiddle factors and hence the ROM memory size is gets shrunken an chip size is reduced. The efficiency of the processor can be improved by reducing its truncation error, mean error and mean square error of the multipliers used these processors by using fixed width modified booth multiplier. Our designed hardware requires about 33.6k gates, and has a working frequency up to 80 MHz synthesized by using 0.18µm CMOS technology. Since our design requires low-cost and consumes low power, as well as reduce the truncation error, SQNR and highly efficient and also adapted to high-point FFT applications.

4. OBJECTIVES

In order to reduce no. of complex multipliers compared to radix 2 algorithm. It is very suitable for applications in implantable or portable devices because of its low area and power consumption ,Higher performance, Saves power and area in portable device. Less no. of multiplication operations. The approach can be implemented for higher radix algorithms. Design requires low-cost and consumes low power ,as well as reduce the truncation error[4]

5. PROBABLE OUTCOMES

FFT generally operates over complex input number and much reaches has been done on the efficient designs for the computations of FFT of complex input samples. The comparison is made in terms of required number of complex multipliers, complex adders, complex delays elements and twiddle factor.[5]

In efforts to limit quantization error the pre-computed offset and step sizes contain additional error bits which are carried throughout the computation and subsequently truncated at the output of the twiddle generator. The number of additional bits is a function of the maximum number of consecutive multiplies at a given twiddle stage. The rounding module used to truncate the output , alternative designs which account for pipelining of the multiplier are feasible; however additional offsets and step sizes must be pre-computed and stored. [3]

6. FUTURE WORK

As, it has been shown the application of FFT is that mathematical analysis of signals .To make it flexible for N point and implement it on real time hardware. In this we will use the parallel multiplier will give output in one clock cycle independent of the number of bits at the input in normal cases form bit multiplier it requires n clock cycle which makes it slow so, for 16 bit clock cycle while in or case output will come in one clock cycle.

REFERENCE

[1] Mario Galvez, J Grajal, M A. Sanchez and Oscar Gustafsson."Pipelined Radix-2(k) Feed Forward FFT Architectures"2013, IEEE Transaction on Very Large Scale Integration (vlsi) Systems

[2] Manohar Ayinala, Keshab K. Parhi**"**Parallel-Pipelined Radix-2^2 FFT Architecture for Real Valued Signals" Department of Electrical and Computer Engineering ,University of Minnesota, Mimmeapolis, Mn, Usa.

[3] K. Jayaram, C. Arun & B. Sakthivel, "Design of parallel pipelined feed forward architecture for zero frequency & minimum computation algorithm of FFT" [1,3]assistant Professor, Department of ECE, Madurai Institute & Technology, Tamil Nadu, India, Professor, Department of ECE, R.M.K College of Engineering & Technology , Tamil Nadu , India.

[4]A.Anbarasan[1], J.Deepa[2], N.Rekha[31]Assistant Professor, SuryaCollege of Engineering, Villupuram.[2]U.G scholar, Surya CollegeofEngineering,Villupuram.[3]U.Gscholar, Surya College ofEngineering,Villupuram,deepa.mary10@yahoo.com."Desig n Of Low Power, High Efficient Fft/IfftProcessor For Wireless Communication"
[5]Anbarasan.A, Shankar.K "Design and implementation of low power FFT/IFFT processor for wireless communication" Proceedings of the International Conference on Pattern Recognition, Informatics and Medical Engineering (PRIME-2012), pp. 152-155, March 2012.
[6] Chu yu, Mao-Hsu Yen " A Low power 64-point FFT/IFFT Processor for OFDM Applications" IEEE Transactions on Consumer Electronics,Vol. 57, Feb 2011.
[7] N.Kirubanandasarathy, Dr.K.Karthikeyan," VLSI Design of Mixed Radix FFT Processor for MIMI-OFDM in Wireless Communication", 2011 IEEE Proceedings
[8] Anbarasan.A, Shankar.K "Design and implementation of low power FFT/IFFT processor for wireless communication" Proceedings of the International Conference on Pattern Recognition, Informatics and Medical Engineering (PRIME-2012), pp. 152-155, March 2012.
[9] Chu yu, Mao-Hsu Yen " A Low power 64-point FFT/IFFT Processor for OFDM Applications" IEEE Transactions on Consumer Electronics,Vol. 57, Feb 2011.
[10] N.Kirubanandasarathy, Dr.K.Karthikeyan," VLSI Design of Mixed Radix FFT Processor for MIMI-OFDM in Wireless Communication", 2011 IEEE Proceedings.
[11] Fahad Qureshi and Oscar Gustafson,"Twiddle Factor Memory Switching Activity Analysis of Radix-2^2 and Equivalent FFT Algorithms", IEEE Proceedings, April 2010.
[12] Jianing Su, Zhenghao Lu, "Low cost VLSI design of a flexible FFT processor", IEEE Proceedings, April 2010.
[13] He Jing, Ma Lanjaun, Xu Xinyu, "A Configurable FFT Processor", IEEE proceeding 2010.
[14] M.Merlyn, "FPGA Implementation of FFT Processor with OFDM Transceiver", 2010 IEEE proceeding.
[15] Nuo Li and N.P.van der Meijs, "A Radix based Parallel pipelined FFT processor for MB- OFDM UWB system," IEEE Proceedings, 2009.
[16] Minhyrok Shin and Hanho Lee, " A High-Speed Four Parallel Radix-2^4 FFT/IFFT Processor for UWB Applications," in Proc. IEEE Int. Symp. Circuits and systems, 2008, pp. 960-963.
[17] Yuan Chen, Yu-Wei Lin, "A Slock scalin FFT/IFFT processor for WiMAX Applications" IEEE proceedings 2006.