
Development and Investigation on an Embedded System Education and Promotion

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Abstract

In today's hi tech and hi precision world, robot finds its application in many areas to carry out operations that are routine, highly complex and critical, hazardous or of high precision nature. Robots when networked offer many benefits such as increased maneuverability and efficiency. This paper makes a survey on the present developmental status and details the design features of networking mobile robots using embedded system based control. It is intended to use this work as basis for future research work in the area of cooperative behavior of mobile robots.

INTRODUCTION

Practical application is an important component of any scientific and engineering research and more so in the field of robotics. The applications of robot in day to day activities for industrial and time critical fail safe operations are increasing. Some of the broader examples are agriculture, automotive manufacturing, construction, entertainment, health care, laboratories, security and surveillance, military, mining, warehouse operations etc. Robot for industrial applications include critical and complex assembly operations which are of repetitive nature, performing routine operations such as pick and place, process control operations in nuclear and robotic arm in space to perform time critical and fail safe operations with minimum human intervention. Applications such as walk ing robot for human health care of elderly or handicapped people and for recreational activities are also on the increase.

A case study is presented to demonstrate the performance of the universal learning system. Three embedded hardware platforms [11] [13] are

imported into the proposed system. For each hardware platform, a short course is carefully designed according to the features of this hardware platform. A user can choose the hardware platform and take the course according to the suggestion of the preference estimation system. The student feedback shows that most students agreed the proposed system could help their study in embedded software design

METHODOLOGY

This work adopt the Harvard architecture shown in Fig. 1, Considering scratchpad memory locates on the same level as the set associative level 1 (L1) instruction cache. While a Agenda consists of a quantity of data and code objects, this revision only consider the plan of code objects. A code object is loaded to SPM or main memory depending on the code layout design . If a code object is Loaded to the main memory, it occupies a number of adjacent memory blocks. Believing that the size of a memory block equals the size of SPM and the cache block size is smaller than the main memory and SPM size.

The proposed system , design a architecture which consists of On chip SPM and cache alone

with external cache which avoid all the cache misses. This external cache is laced between the main memory and On chip. Any miss in SPM or internal cache will direct the search to external cache instead of going to the main memory which will save the energy and advance the performance. Scratch Pad Memory is simple SRAM memory placed on chip along with the processor. SPM consumes less CPU cycle and energy, unlike the main memory the size of the scratchpad memory is limited to be a fraction of the total application size.

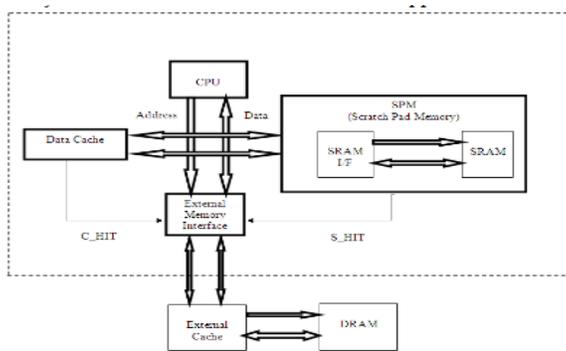


Fig1: Architecture Diagram

A SCRATCH PAD MEMORY

Software managed memory such as scratch pad memories are important particularly in case of image and video processing application where heavy use of multi dimensional array is implemented. As these applications need large area for its storage, scratch pad architectures are used, which results in large saving in energy and improvement in the efficiency of the system.

Scratch pad memory based system uses, the programmer or the compiler who are responsible for scheduling the data Transfer between the SPM and the off chip memory. Effective scheduling of memory will improve both the efficiency and performance of the application.

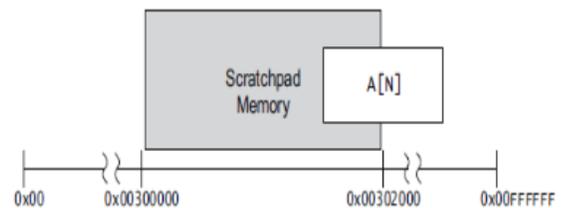


Fig 2: Processor Address Space Containing a Scratchpad Memory

In most of the embedded systems scratch pad memory occupy small portion of the memory address space [1]. Figure 2 shows a setup in which the scratchpad occupies a 4k address region ([0x00300000, 0x00302000]) from the processor's address space ([0x00000000, 0x00FFFFFF]). Any access to the 4k address region is translated to a scratchpad access, whereas any other address access is mapped to the main memory

Multidimensional Scaling

In the previous section, we use quantified feature vectors to construct the dissimilarity matrix, which shows the degree of similarity among different hardware kits. Nevertheless, a user still has to spend lots of time searching for the relationship from this $k \times k$ matrix, so a friendly interface to present this relationship is necessary, such that users can read this dissimilarity matrix with ease

EXPERIMENTAL RESULTS

The section evaluates the effectiveness of code repositioning, SPM code selection, Cache code selection and combined benefit of both along with external cache. The first section describes the simulation setting, while the Next compare the power reduction and memory access distribution of benchmark programs. Thus, this section compares code layout schemes determined using different methods code repositioning for cache and SPM configuration initially fetches the instruction for application. The searching of the data is done in cache, some energy is consumed for accessing the cache memory. If the data is present in the cache then the process will start,

else the process will go for the SPM to get the data. So the energy will be consumed for accessing the SPM. Thus without accessing the Main memory the instruction is processed. This leads to the less consumption of energy, because for accessing the main memory only the energy will be consumed more. Same is done for single and multiple processors along with dynamic and static SPM and comparison graph is obtained

PREFERENCE ESTIMATION SYSTEM

The spirit of the universal learning System is the preference estimation system. Before learning embedded systems, the most important thing is selecting a correct hardware kit that corresponds to the user requirements. In this section, we describe the components of the preference estimation system, which has several features:

- Extraction of features from a hardware kit for users.
- Visualization of the relationship between hardware kits.
- Visualization of the user preference.
- Suggestion of suitable hardware kits for users.

Figure 2 illustrates the flow chart of visualizing the hardware features and user preference. In the proposed system, every hardware kit is mapped to a point in a low dimensional coordinate system, such as a 3D cube, 2D plane, or even a 1D line, where the distance between two points illustrates how similar they are. For this purpose, we have to extract the features of every hardware kit first, and then transform these features to a feature vector. After normalization and weight scaling, these feature vectors are used to measure the distance between each other. Here the Euclidean distance is applied to represent the degree of similarity between two feature vectors. Then we can get a dissimilarity matrix describing the relationship between each

pair of feature vectors. However, it is still inconvenient for users to search for relationship in this big matrix, so we use multidimensional scaling [14] to transform the relationship to a low dimensional point, so that users can easily understand this relationship. In the following subsections, the details of every step are described

Feature Extraction

In order to select a suitable hardware kit, a user may need to collect the specifications and spend much time comparing different hardware kits. It is a difficult task especially for a beginner. To help users make comparisons and decisions, the proposed system collects useful information and extracts features for every hardware kit. These features can be classified as three categories, indicating the general information, complexity, and user experience of a hardware kit, respectively. Several objective and subjective feature factors are included to form a feature vector, listed as follows:

CONCLUSION

In this article, the idea of the universal learning system is proposed. The visualization of the dissimilarity matrix lets users intuitively understand the relationship between the hardware platforms and user preference, and helps users select the most suitable hardware platform to learn embedded systems online. In addition to online courses and virtual platforms, users can also join discussions and ask questions using the proposed system. In the demonstration, we applied three hardware platforms used for embedded system education in Taiwan. The results show that users can easily select the most suitable hardware platform and take courses according to requirements. Therefore, the proposed system can help users learn embedded systems anytime and anywhere.

However, there are still some problems in the proposed system. For example, there should be a well organized management for the forum . Also, it is difficult to build up the virtual platform for each hardware platform. In the future, these issues will be taken into account gradually, such that the universal learning system can be more practical

REFERENCES

- [1] ICT Results (2009). ICT and innovation: From micro chips to macro solutions [Online] a available at <http://cordis.europa.eu/ictresults/index.cfm?section=news&tpl=brochures> report.
- [2] C. - S. Lee, J.-H. Su, K.-E. Lin, J.-H. Chang, and G.-H. Lin, "A project based laboratory for learning embedded system design With Industry Support," IEEE Transactions on Education , vol. 53, no. 2, pp. 173 181, May 2010.
- [3] S.H. Kim and J.W. Jeon, Introduction for Freshmen to Embedded Systems Using LEGO Mindstorms IEEE Transactions on Education Vol 52, No 1, pp. 99 to 108.W. -K, Feb. 2009
- [4] M. Winzker and A. Schwandt, "Teaching embedded system concepts for technological literacy," IEEE International Conference on Microelectronic Systems Education , pp. 89 -92, 2009.
- [5] D.T. Rover, R.A. Mercado, Z. Zhang, M.C. Shelley, and D.S. Helvick, " Reflections on Teaching and Learning in an Advanced Undergraduate Course in Embedded Systems " IEEE Transactions on Education , Vol 51, No 3, pp. 400 -412, Aug. 2008.
- [6] J. - S. Chenard, Z. Zilic, and M. Prokic, A Laboratory Setup and Teaching Methodology for Wireless and Mobile Embedded Systems" , IEEE Transactions on Education , Vol 51, No 3, pp. 378 - 384, Aug. 2008.
- [7] J. O. Hamblen, "Using a low cost SoC computer and a commercial RTOS in an embedded systems design course," IEEE Transactions on Education , vol. 51, no. 3, pp. 356 -363, August 2008.
- [8] T. Tierens, P. Pelgrims, W. Dams, and P. V. Pelt, "Interdisciplinary embed ed system design in education," IEEE International Conference on Microelectronic Systems Education , pp. 135 - 136, 2007.
- [9] S. Nooshabadi and J. Garside, Modernization of Teaching in Embedded Systems Design An International Collaborative Project IEEE Transactions on Education , Vol 49, No 2, pp. 254 to 262, May. 2006.
- [10] National Chip Implementation Center, Taiwan. Available At <http://www.cic.org.tw>
- [11] Sunplus Technology Co. Ltd. , a available at <http://www.sunplus.com>
- [12] ANDES Technology Co. Ltd. , a available at <http://www.andestech.com>
- [13] Industrial Technology Research Institute, Taiwan , a available at <http://www.itri.org.tw>
- [14] Borg and P. Groenen, Modern Multidimensional Scaling: theory and applications (2nd ed.) , New York: Springer - Verlag pp. 207 – 212 , 2005.
- [15] R. M. Branch, Instructional design: the ADDIE approach, New York: Springer, 2010.
- [16] S. Smaldino, D. Lowther, and J. Russell, Instructional media and technologies for learning, 9 ed., Englewood Cliffs: Prentice Hall, Inc, 2007.
- [17] R. H. Dave, Developing and writing behavioral objectives, R. J. Armstrong, ed., Tucson, Arizona: Edu cational Innovators Press, 197