VLSI IMPLEMENTATION OF INTEGER DCT ARCHITECTURES FOR DEVELOPMENT OF LOW TEMPERATURE OXIDATION

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Abstract

With decreasing size of MOS transistor the thickness of gate oxide (SiO_2) is reaching in regime where it is just 2 - 3 atomic layers thick about 1 to 1.5 nm thick because of thin oxide layers there is direct tunnelling of charge carriers through gate oxide, and the transport of charge carriers through defects in gate oxide. The increasing leakage urrent through gate oxide is proving to be a showstopper to the scaling of MOS transistor, and saturating the Moore's Law. For the applications, where the devices are need to be fabricated on plastic, glass or poly crystalline silicon substrates a good quality of oxide is required to be grown at low temperatures. In this work a low temperature, defect free oxide growth technique using ozone is presented and we study the effect of various ambient temperatures on growth of SiO_2, the effect of pre cleaning and passivation on quality of ozone grown oxide in terms of bulk defect density, Si-SiO_2 interface trap charge density and on oxide life time is presented.

Introduction

High Efficiency Video Coding (HEVC) inverse transform for residual coding uses 2 -D 4x4 to 32x32 transforms with higher precision as compared to H.264/AVC's 4x4 and 8x8 transforms resulting in an increased hardware complexity. In this paper, an energy and area - efficient VLSI architecture of an HEVC - compliant inverse transform and dequantization engine is presented. We implement a pipelining scheme to process all transform sizes at a minimum throughput of 2 pixel/cycle with zero-column skipping for improved throughput. We use data - gating in the 1-D Inverse Discrete Cosine Transform engine to improve energy - efficiency for smaller transform sizes. A high - density SRAM - based transpose memory is used for an area - efficient design. This design supports decoding of 4K Ultra - HD (3840x2160) video at 30 frame/sec. The inverse transform engine takes 98.1 kgate logic, 16.4 kbit SRAM and 10.82 pJ/pixel while the dequantization engine takes 27.7 kgate logic, 8.2 kbit SRAM and 1.10 J/pixel in 40 nm CMOS technology. Although larger transforms require more computation per coefficient, they typically contain a smaller proportion of non - zero coefficients. Due to this trade off, larger transforms can be more energy efficient.

HEVC Coding Design and Feature Highlights

The HEVC standard is designed to achieve multiple goals, including coding efficiency, ease of transport system integration and data loss resilience, as well as implementability using parallel processing architectures. The following subsections briefly describe the key elements of

the design by which these goals are achieved, and the typical encoder operation that would generate a valid bit stream. possible implementations of integer DCT for HEVC in the context of resource requirement
and reusability, and based on that, we have derived the proposed algorithm for hardware indentation. We have designed scalable and reusable architectures for 1-D and 2-D integer DCTs for HEVC that could be reused for any of the prescribed lengths with the same throughput of processing irrespective of transform size.

Video Coding Layer

The video coding layer of HEVC employs the same hybrid approach (inter-/intrapicture prediction and 2-D transform coding) used in all video compression standards since H.261. Fig. 1 depicts the block diagram of a hybrid video encoder, which could create a bitstream conforming to the HEVC standard.

The oxidation process of silicon is the heart of all the fabrication steps followed in fabricating a MOSFET and makes a MOFET functional. But with the advancement in the IC technology and diminishing size of MOSFET's this crucial SiO2 is getting thinner and thinner. The thickness of SiO2 currently required is less than 1 nm [1], which is just 3 monolayer of SiO 2 (1 monolayer ~ 0.3nm). For the performance evaluation MOSFETs, the most basic factor is the current between source and drain, which the transistor is able to drive. More current shows that the transistor can be operated faster and all the parasitic capacitances and resistances within that transistor are having a lesser impact on MOSFET. Firstly, the gate voltage, applied between gate electrode and substrate separated by a dielectric material to form a parallel plate capacitor type arrangement, and the accumulation or inversion of the charge carriers is induced in the substrate on its application. The higher performance demanded from the transistor. From the basics of the MOSFET operation; we know there are two voltages available to control the operation of the value of capacitance signifies more inversion charge carriers in the semiconductor channel for the same applied voltage. And the second one is the voltage, which we apply between source, and drain, which is accountable for driving the induced charges forward in the channel. Thus SiO2is the dielectric material, which made FET transistors to work in silicon technology.

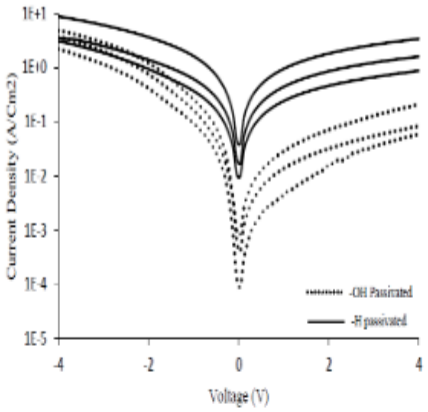

Fig. 1 Gate leakage current density for different devices of area 7.78e-3 cm^2 distributed across wafer.

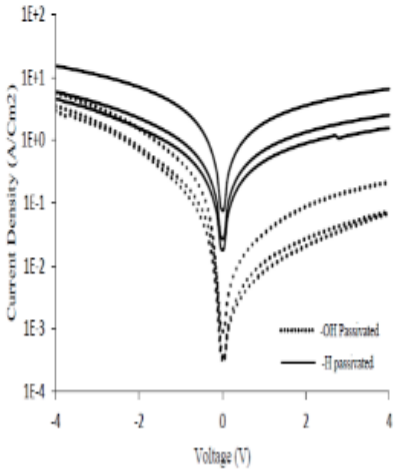

Fig. 2 Gate leakage current density for different devices of area 4.62e-3 cm^2 distributed across wafer.

We know that both –H and –OH covered silicon surface shows an initial repulsion to the O_3molecule and thus initially cause a little inhibition in SiO_2 growth. But from the differences in the final optical thickness that we have measured, it can be concluded that –OH ions provide more inhibit ion for SiO2 growth. We have deduced the level of bulk defects present in both the oxides from J -V curves of devices of different dot areas for both type of passivation as the gate leakage is dependent on two factors 1) Tunneling of charge carriers 2) Conduction through bulk defects. The behaviors shown by leakage current density for small and large area devices shows that for large area devices the defect assisted leakage is prominent as compared to tunneling component of current in –H passivated devices even though the thickness is high as compared to –OH passivated but since defects are randomly distributed over area and thus the defect associated component is decreased with area and since tunneling is high in –OH passivated, for small areas the leakage current is high in –OH passivated.

An encoding algorithm producing an HEVC compliant bit stream would typically proceed as follows. Each picture is split into block-shaped regions, with the exact block partitioning being conveyed to the decoder. The first picture of a video sequence (and the first picture at each clean random access point into a video sequence) is coded using only intra picture prediction (that uses some prediction of data spatially from region-to-region within the same picture, but has no dependence on other ictures). For all remaining pictures of a sequence or Between random access points, intermixture temporally predictive coding modes are typically used for most blocks. The encoding process for inter picture prediction consists of choosing motion data comprising the selected reference picture and motion vector (MV) to be applied for predicting the samples of each block. The encoder and decoder generate identical inter picture prediction signals by applying motion compensation (MC) using the MV and mode decision data, which are transmitted as side information.

The residual signal of the intra-or interpicture prediction, which is the difference between the original block and its prediction, is transformed by a linear spatial transform. The transform coefficients are then scaled, quantized, entropy coded, and transmitted together with the prediction information. The encoder duplicates the decoder processing loop (see gray-shaded boxes in Fig. 1) such that both will generate identical predictions for subsequent data. Therefore, the quantized transform coefficients are constructed by inverse scaling and are then inverse transformed to duplicate the decoded approximation of the residual signal. The residual is then added to the prediction, and the result of that addition may then be fed into one or two loop filters to smooth out artifacts induced by block-wise processing and quantization. The final picture representation (that is a duplicate of the output of the decoder) is stored in a decoded picture buffer to be used for the prediction of subsequent pictures. In general, the order of encoding or decoding processing of pictures often differs from the order in which they arrive from the source; necessitating a distinction between the decoding order (i.e., bitstream order) and the output order (i.e., display order) for a ecoder. Video material to be encoded by HEVC is generally expected to be input as progressive scan imagery (either due to the source video originating in that format or resulting from deinterlacing prior toencoding). No explicit coding features are present in the HEVC design to support the use of interlaced scanning, as interlaced scanning is no longer

used for displays and is becoming substantially less common for distribution. However, a metadata syntax has been provided in HEVC to allow an encoder to indicate that interlacescanned video has been sent by coding each field (i.e., the even or odd numbered lines of each video frame) of interlaced video as a separate picture or that it has been sent by coding each interlaced frame as an HEVC coded picture. This provides an efficient method of coding interlaced video without burdening decoders with a need to support a special decoding process for it.

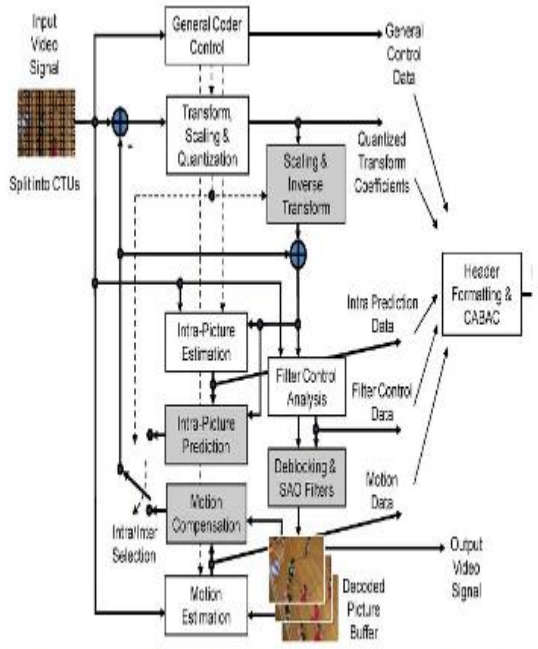

Fig. 1. Typical HEVC video encoder (with decoder modeling elements shaded in light gray).

Algorithm for Hardware Implementation of Integer DCT for HEVC:

In the Joint Collaborative Team-Video Coding (JCT-VC), which manages the standardization of HEVC, Core Experiment 10 (CE10) studied the design of core transforms over several meeting cycles. The eventual HEVC transform design involves coefficients of 8-bit size, but does not allowfull factorization unlike other competing proposals. It however allows for both matrix multiplication and partial butterfly implementation. In this section, we have used the partial-butterfly algorithm of for the computation of integer DCT along with its efficient algorithmic since it has two 1-D DCT units and nearly the same complexity of transposition buffer while the throughput of full-paralleldesign is double the throughput of folded design. Thus, thefull-parallel design involves 15.6% less EPS We also synthesized the the folded and Full -parallel structures for 2-D integer DCT. We have listed total gate counts,processing rate, throughput, power consumption, and EPS in Table VII. We set the operational frequency to 187 MHz For both cases to support UHD at 60 frames/s. The 2-D full-parallel structure yields 32 samples in each cycle after initial latency of 32 cycles providing double the throughput of the folded structure. However, the full -parallel architecture consumes 1.69 tim
es more power than the folded architecture

CONCLUSION

In this paper, we presented a very low-complexity DCT approximation obtained via pruning. The resulting approximate transform requires only 10 additions and possesses performance metrics comparable with state-Of -the-art methods, including the recent Architecture presented in [24]. By means of computational simulation, VLSI hardware realizations, and a full HECV implementation, we demonstrated the practical relevance of our method as an image and video codec
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