A New Algorithm for ARM7 Processor in Embedded systems to implement conventional encoder

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***Abstract*_-In digital communication Convolution encoder and Viterbi decoder are widely used due to the excellent error control performance. The most popular communications decoding algorithm, the Viterbi Algorithm (VA), requires an exponential increase in hardware complexity to achieve greater decode accuracy. The path associated with the input bits are large, hence it needs to implement the path memory with lesser hardware for lesser computations to decode the original data. When the decoding process uses the Modified Viterbi Algorithm (MVA) computations are reduced to 50% thereby reduction in the hardware utilization, which follows the maximum-likelihood path. This work focuses on the realization of convolutional encoder and modified Viterbi decoder (MVD) with a constraint length, K of 3 and a code rate (k/n) of 1/2 using Field Programmable Gate Array (FPGA) technology.**

***Keywords*--Convolutional Encoder, Modified Viterbi Algorithm (MVA), Verilog HDL, FPGA**

I INTRODUCTION

Convolutional coding with Viterbi decoding [1] is a powerful method for forward error correction. In today's digital communications, the reliability and efficiency of data transmission is the most concerning issue for communication channels. Error correction technique plays a very important role in communication systems. The error correction technique improves the capacity by adding redundant information for the source data transmission. All communication channels are subject to the additive noise. Forward error correction (FEC) techniques are used in the transmitter to encode the data stream and receiver to detect and correct bits in errors, hence minimize the bit error rate (BER) to improve the performance. RS decoding algorithm complexity is relatively low and can be implemented in hardware at very high data rates. It seems to be an ideal code attributes for any application. However, RS codes perform very poorly in additive noise. Due to weaknesses of using the block codes for error correction in useful channels, another approach of coding called convolutional coding had been introduced in 1955 [1]. Convolutional encoding with Viterbi decoding is a powerful FEC technique that is particularly suited to a channel in which the transmitted signal is corrupted mainly by additive white Gaussian noise (AWGN) [2]noise. It operates on data stream to encode. It is simple and has good performance with high implementation cost. But the implementation requires the exponential increase in the area and power consumption to achieve increased decoding accuracy.

So we introduce modified viterbi decoder with memory. Modified Viterbi [3], decoders are used to decode Convolutional codes. In most of real time applications like audio/video and recently in digital wireless communications, the Convolutional codes are used for error correction. It is very efficient and robust. The main advantage of Modified Viterbi Decoder is it has fixed decoding time and also it suites for hardware decoding implementation.

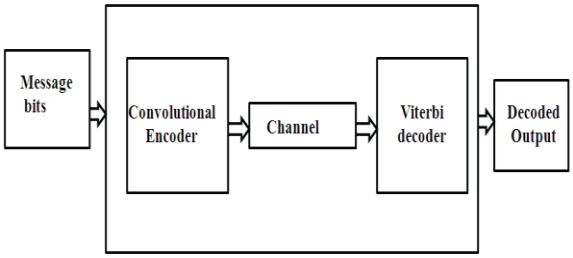
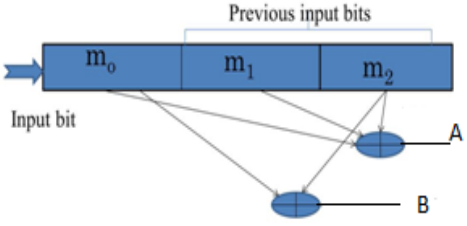


Figure: 1 Basic Block Diagram

II CONVOLUTIONAL ENCODER

Convolutional codesare frequently used to correct errors in noisy channels. They have rather good correcting capability and perform well even on very bad channels (with error probabilities of about (10^{-3}) [4]. Convolutional codes are extensively used in satellite communications. Although convolutional encoding is a simple procedure, decoding of a convolutional code is much more complex task.



Where A, B are outputs.

Figure: 2 Convolutional encoder.

Convolutional Encoder shown in Figure2 takes input data bit and gives out two bits. Convolutional encoding is a process of adding redundancy to a signal stream. To convolve the encode data; start with 2 memory registers, each holding 1 input bit. Registers start with a value of 0. The encoder has 2 modulo-2 adders which are implemented with a XOR gate. It generates 2 bit polynomials, one for each adder.

A=m0 ***XOR*** m1 ***XOR*** m2
B=m0 ***XOR*** m2

The convolutional encoder is basically a finite state machine [5].The k bit input is fed to the constraint length K shift register and the n outputs are calculated from the generator polynomials by the modulo-2 addition. Encoder functions depending on the applied input, and then the corresponding state transition takes place. The function of encoder understood with the help of the following state diagram. These state diagrams generally implemented with the sequential circuits based on the constraint length [6] used at the transmitter side.

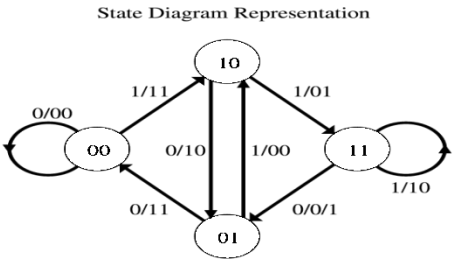


Figure: 3 State diagram of convolutional encoder.

State diagram: This offers a complete description of the system. However, it shows only the instantaneous transitions. It is illustrate in the *State table* as fallows

	Next State, if	
Current State	**Input = 0:**	**Input = 1:**
00	00	10
01	00	10
10	01	11
11	01	11

Figure: 4 State table for next state of convolutional encoder

	Output Symbols, if	
Current State	**Input = 0:**	**Input = 1:**
00	00	11
01	11	00
10	10	01
11	01	10

Figure: 5 State table for output symbols of convolutional encoder.

III. VITERBI ALGORITHM

The Viterbi decoding algorithm is a decoding process for convolutional codes in memory-less noise channel [7]. The algorithm can be applied to a host of problems encountered in the design of communication systems. The Viterbi Algorithm (VA) finds the most-likelihood path transition sequence in a state diagram, given a sequence of symbols,

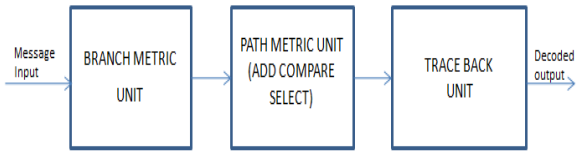


Figure:6 Block diagram of viterbi decoder.

A Viterbi algorithm consists of the following three major parts:

A. Branch metric calculation

The first unit is called branch metric unit. Here the received data symbols are compared to the ideal outputs of the encoder from the transmitter and branch metric is calculated by performing the XOR operation, thereby counting the number of ones.

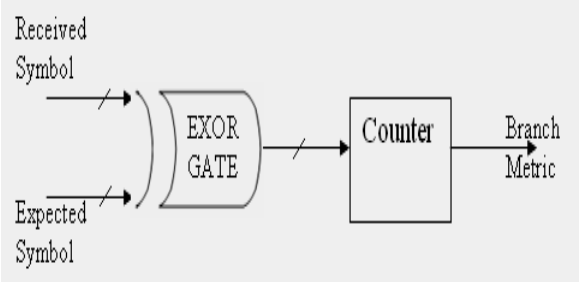


Figure: 7 Branch metric calculation

B. Path metric calculation

For every encoder state, calculate a metric for the Survivor path *ending* in this state (a survivor path is a path with the minimum metric).it is per formed by Add Compare Select Unit.

Add Compare Select

The function of ACS is completing survivor paths and generating decision vector, and the whole computation process includes add operation, compare operation, and select operation. By analysis on accumulation process, can find that each branch metric value is non-negative. So the branch accumulation metric value is continually incremental, in case the accumulator overflows, so there is a normalization function. This function means that every time the accumulation metric value of each state must subtract the minimum of all accumulation metric values. The structure of ACS is shown in the Figure below.

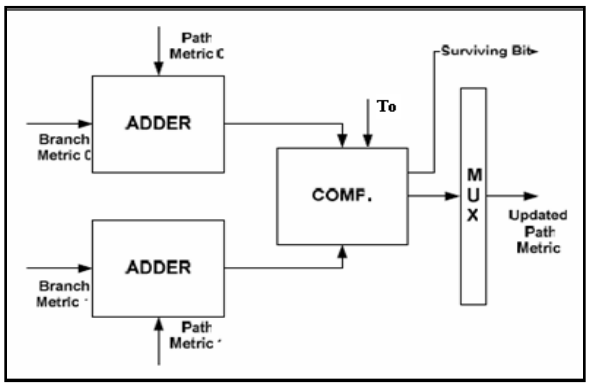


Figure: 8 Add Compare Select Unit.

C. Trace back unit

This step is necessary for hardware implementations that don't store full information about the survivor paths, but store only one bit decision every time when one survivor path is selected from the two.

IV MODIFIED VITERBI ALGORITHM

The average computation and path storage required by the MVA are reduced [3]. Instead of computing and retaining all 2K-1 possible paths, only those paths which satisfy certain cost conditions are retained for each received symbol at each state node here we have path memory to store the total path of the input and output.

Survivor Path unit

The survivor path unit stores the decisions of the ACS unit and uses them to compute the decoded output. The trace-back technique and the register-exchange approaches are two major techniques used for the path history management .The Trace back unit takes up less area but require much more time than the Register Exchange method.

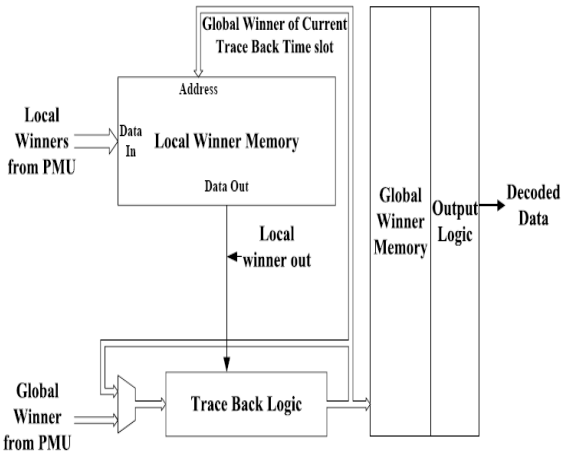


Figure: 9 Survior path unit with path memory

In figure 9 the operation performed is the shortest path obtained from the local memory is stored in the trace back unit. Then it is compared with the shortest path from the global winner memory and the shortest is replaced in the global winner memory.

V. SIMULATION OF VITERBI ALGORITHM

The various modules of Convolutional encoder and Viterbi decoder in verilog HDL is implemented here. The whole process of convolutional encoder and Modified Viterbi decoder can be summarized as shown in the flowchart shown in figure10.

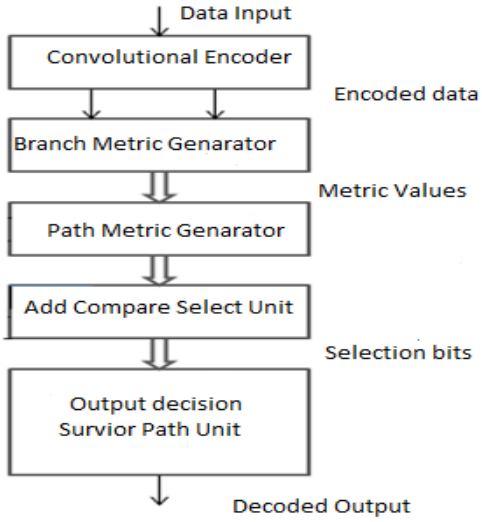


Figure: 10 Flowchart of the convolutional encoder and viterbi decoder

VI. EXPERIMENTAL RESULTS

The function of convolutional encoder and Viterbi decoder can be observed by manually in Isim simulator. The "clk"is the clock signal of whole system, and the reset is the reset signal of whole system. When the reset is set high, the convolution encoder and Viterbi decoder begin to work. The"inp" and "out" respectively stand for input signals to convolution encoder and output signals. The results are obtained as follows.

A. CONVOLUTIONAL ENCODER

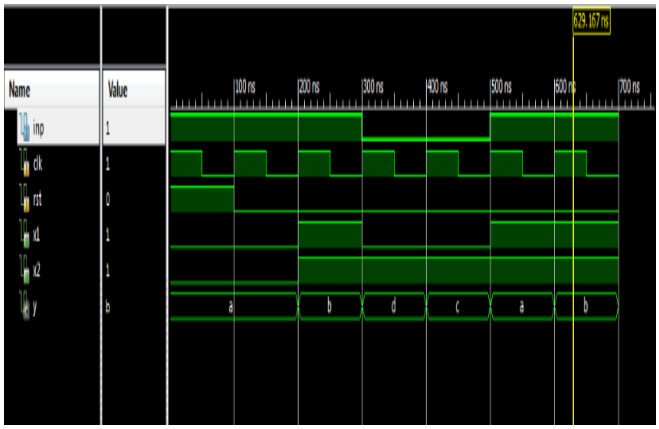


Figure: 11 Simulation results of convolutional encoder**.**

In figure 11 the initial input given is "1" previous states are "0" and"0" respectively. And initial at "00" state, then based on the output and in accordance to the state diagram the next state is assigned.

B. BRANCH METRIC UNIT

The branch metric and path metrics calculation is shown in the simulation figure 12 and figure 13respectively.

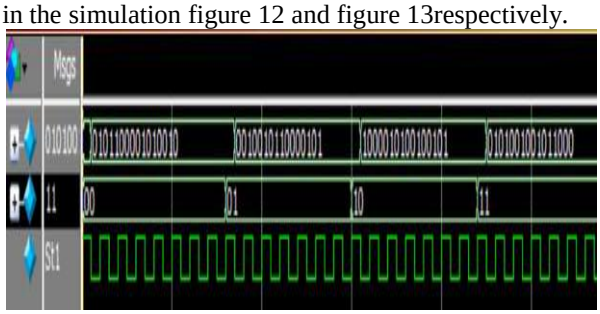


Figure.12. Simulation result of Branch Metric Unit.

In figure 12 the output obtained from the convolutional encoder is taken and XOR operation is performed and if the output is "1" counter status will be incremented by "1".

C. PATH METRIC UNIT

In figure 13 the operation performed is, the output obtained from the branch metric unit are compared at each and every node and the node with highest metrics is obtained from the multiplexer.

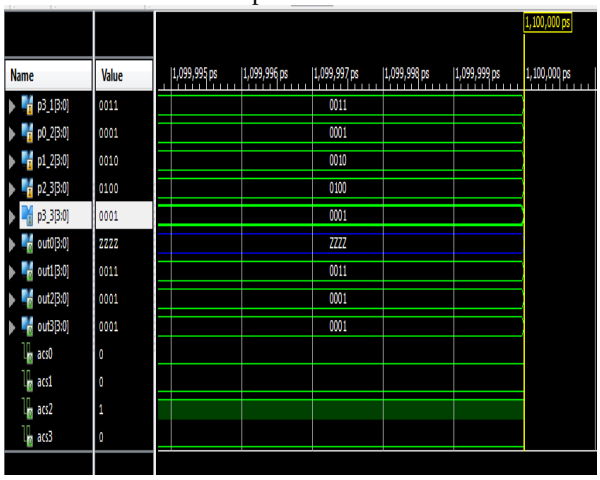


Figure. 13. Simulation result of Path Metric Unit

D. VITERBI DECODER

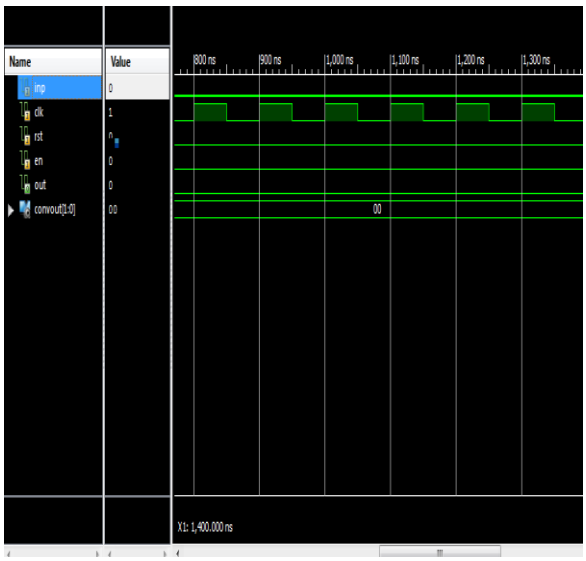


Figure: 14 Simulation results of viterbi decoder**.**

The figure 14 shown is the output of viterbi decoder which consists of large number of Add Compare Select Units the initial input given is "0" and the output obtained is also "0".

E.MODIFIED VITERBI DECODER

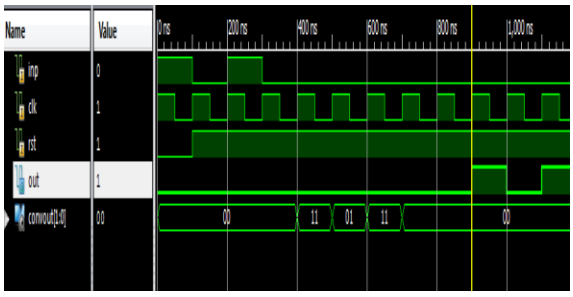


Figure: 15 Simulation result of modified viterbi decoder.

From the experimental results, it is clear that the input signal to the convolution encoder is identical to the output signal from the Viterbi decode. The input data is given to the encoder and from which the encoded data is given to the viterbi decoder and it performs all the operations in it. And after the decoding time, the decoded data is obtained and is similar to the original input data. The simulation result of the modifiedviterbi decoder operation is shown in above figure. The input sequence "10100"is given to the convolutional encoder and the final output obtained from the modified viterbi decoder is also "10100" after a delay of 6 clock cycles.

VII COMPARISION OF TWO DECODERS

(Estimated values)

Logic Utilization	Viterbi Decoder	Modified Viterbi Decoder
Number of slices	**499**	**59**
Number of slice flip flops	**404**	**29**
Number of 4 input LUTs	**898**	**108**

Figure: 16 Comparison of viterbi decoder and modified viterbi decoder in design summary.

This shows that viterbi decoder occupies the area almost 50 times more than that of modified viterbi decoder. So the power required for viterbi decoder will also be more than that of modified viterbi decoder since the number of Add Compare Select Units are reduced in the modified viterbi decoder. So, modified viterbi decoder is more efficient than viterbi decoder.

VIII. CONCLUSION

Here the convolutional encoder, viterbi decoder and modified viterbi decoder are implemented. This design has been simulated in Isim and synthesized using XILINX-ISE 12.2a for the given input sequence and shown that modified viterbi decoder is moresuited to a channel in which transmitted signal is corrupted mainly by additive white Gaussian noise (AWGN).At the same time, the look-up table requirements are kept to a minimum. Thus the area utilized is reduced and thereby low power consumption can be achieved. The future work is focused on design a variable convolution encoder and Viterbi decoder. Because a variable convolution encoder and Viterbi decoder has a better flexibility in application.

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