A Review on "CMOS Full-Adders Using Arithmetic Applications"

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ABSTRACT

Two high-speed and low-power full-adder cells designed with an alternative internal logic structure and pass-transistor logic styles that lead to have a reduced power-delay product (PDP). We carried out a comparison against other full-adders reported as having a low PDP, in terms of speed, power consumption and area. All the full-adders were designed with a 0.18µm CMOS technology, and were tested using a comprehensive testbench that allowed to measure the current taken from the full-adder inputs, besides the current provided from the power-supply. Post-layout simulations show that the proposed full-adders outperform its counterparts exhibiting an average PDP advantage of 80%, with only 40% of relative area.

Key words: Arithmetic, full-adder ,high-speed, low power

1. INTRODUCTION:

Energy-Efficiency is one of the most required features for modern electronic systems designed for high-performance and/or portable applications. In one hand, the ever increasing market segment of portable electronic devices demands the availability of low-power building blocks that enable the implementation of long-lasting battery-operated systems. On the other hand, the general trend of increasing operating frequencies and circuit complexity, in order to cope with the throughput needed in modern high-performance processing applications, requires the design of very high-speed circuits. The power-delay product (PDP) metric relates the amount of energy spent during the realization of a determined task, and

stands as the more fair performance metric when comparing optimizations of a module designed and tested using different technologies, operating frequencies, and scenarios.

Addition is a fundamental arithmetic operation that is broadly used in many VLSI systems, such as application-specific digital signal processing (DSP) architectures and microprocessors. This module is the core of many arithmetic operations such as addition/subtraction, multiplication, division and address generation. As stated above, the PDP exhibited by the full-adder would affect the system's overall performance .Thus, taking this fact into consideration, the design of a full-adder having low-power consumption and low propagation delay results of great interest for the implementation of modern digital systems.

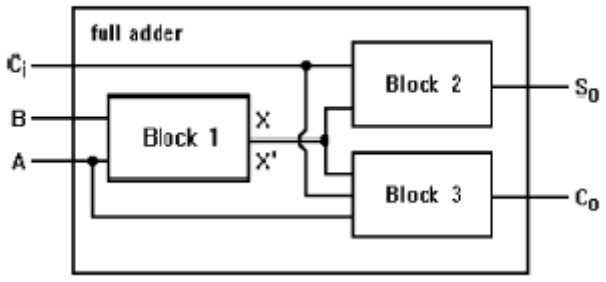

Figure 1 Full-adder cell formed by three main logical blocks.

Full adder is combinational circuits that forms the arithmetic sum of three inputs bits. In full adder there is a three inputs and two ouputs. In our block diagram we use three inputs as A, B, Ci. The third input is carry input. The outputs are SUM and CARRY.

2. REVIEW

Many papers have been published regarding the optimization of low-power full-adders, trying different options for the logic style standard CMOS, differential cascode voltage switch (DCVS) , complementary pass-transistor logic (CPL), double pass-transistor logic (DPL), swing restored CPL (SR-CPL), and hybrid styles, and the logic structure used to build the adder module . The internal logic structure shown in has been adopted as the standard configuration in most of the enhancements developed for the 1-bit full-adder module. In this configuration, the adder module is formed by three main logical blocks: a XOR-XNOR gate and XOR blocks or multiplexers to obtain the SUM and CARRY outputs (Blocks 2 and 3).[7]. The test bed used for the performance analysis of the full-adders. This simulation environment has been used for comparing the full-adders analyzed in, with the addition of the inverters at the outputs. The size of the input buffers lets to experience some degradation in the input signals, and the size of the output buffers equals the load of four small inverters for this

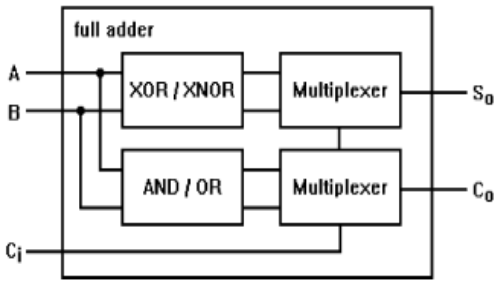

Figure 2 Alternative logic scheme for designing full-adder cells.

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C	B	A	So	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Truth Table of a Full Adder

There are not signals generated internally that control the selection of the output multiplexers. Instead, the C input signal, exhibiting a full voltage swing and no extra delay, is used to drive the multiplexers, reducing so the overall propagation delays. The capacitive load for the C input has been reduced, where the diffusion capacitance is becoming very large for sub-micrometer technologies. Thus, the overall delay for larger modules where the C signal falls on the critical path can be reduced. The propagation delay for the So and Co outputs can be tuned up individually by adjusting the XOR/XNOR and the AND/OR gates this feature is advantageous for applications where the skew between arriving signals is critical for a proper operation etc. Automatic emotion recognition from EEG signals is receiving more attention with the development of new forms of human-centric and human-driven interaction with digital media.

3. OBJECTIVE OF WORK

- The main Aim is to implement CMOS Full-Adders Using Arithmetic Applications for Energy-Efficient. Comparison of two full-adder cells.
- The internal logic structure for designing a full-adder cell.
- The alternative internal logic structure to build the two proposed full-adders.
- Features of the simulation environment used for the comparison.
- Results obtained from the simulations.

4. CONCLUSION

An another internal logic structure for designing full adder cells was introduced. In order to demonstrate its advantages, two full adders were built in combination with pass transistor logic style. For conceived many full adders we can use adder categorization and hybrid design style.

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