A New Theory of Low Power FIR Filter Design Using APC-OMS Algorithm

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Abstract

Memory based structures are used in many kind of digital signal processing (DSP) application. Memory-based structures are better performance In area minimization compare with multiply-accumulate structures and have many other advantages like reduced latency since the memory-access-time is much shorter than the usual multiplication-time compared to the conventional multipliers. The multiplier uses LUT's as memory for their computations. The anti-symmetric product coding (APC) and odd- multiple-storage (OMS) techniques were used for look-up-table (LUT) in adaptive FIR filter. Memory-based structure such as APC and OMS techniques are used for efficient Multiplication. Hence, the combination of these two techniques provides reduction in LUT size to one fourth in adaptive FIR filter when compared with the conventional Look up Table (LUT) of adaptive FIR filter.

INTRODUCTION

Finite impulse response (FIR) digital filters are recent years, DA-based FIR filter has gained substantial common components in many digital signal processing popularity as a primary DSP operation and are rapidly (DSP) systems [1-10]. Throughout the years, with the replacing classic analog filters. increasingly development in very large scale integration (VLSI) technology, the real time realization of FIR filter Algorithm: DA is an important FPGA technology. We with less hardware requirement and less latency has briefly outline here the conventional DA approach for become more and more important. Because the complexity inner product computation [11, 13]. Here is the detail of of implementation grows with the length of filter, several DA. To understand the DA design paradigm [11], algorithms have been made to develop effective consider the ''sum of products'' inner product shown architectures for realization of FIR filters in application below specific integrated circuits (ASIC) and field programmable gate arrays (FPGA) platforms and one of them is (1) distributed arithmetic (DA). The main portion of DAbased computation is lookup table (LUT) that stores the Assume further that An is known constants and xn pre-computed values and can be read out easily, which is a variable [11]. An unsigned DA system assumes that makes DA-based computation well suited for FPGA the xn is represented by realization, because the LUT is the basic components of FPGA.

If the boundary shift adders are replaced by the pipelined shift-adder tree, there will be B-1 number of adders and the latency is log2 B cycle periods. Thus, the latency of the 2-D structure in Ref. [8] is reduced significantly, especially when B is a large number. And the modified architecture is shown in Fig. 1. Moreover, we can also change the systolic array adders of the architecture into the pipelined adder trees, as shown in Fig. 2. Therefore, the whole latency of the architecture is reduced significantly, as well as the number of adders. Since the architecture in Fig. 4 processes all bits of one input word per clock, the architecture can be used for high speed implementation

Implementation of the function Anxn,b requires special attention [11]. The preferred implementation method is to realize the mapping Anxn,b using one LUT [11]. That is, a 2N-word LUT is preprogrammed to accept an N-bit input vector xb and output Anxn,b [11]. The individual mappings Anxn,b are weighted by the appropriate

power-of-two factor and accumulated. After N look-up cycles, the inner product y is computed. Finally, the detail of LUT is shown in Table 1. Moreover, Fig. 1 [11] shows an original LUT-based DA implementation of a 4-order FIR filter.

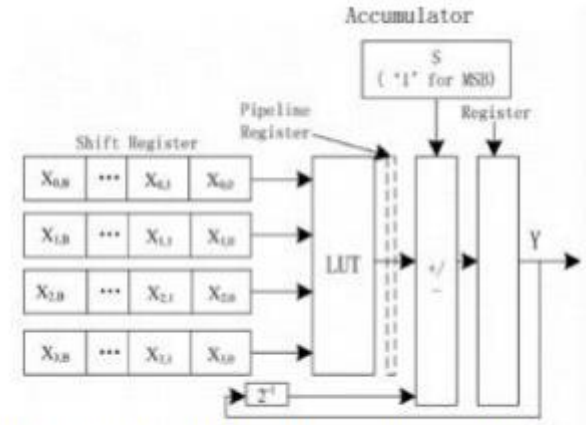

Fig. 1: FIR filters implementation with single LUT.

Modified DA Solutions: Following the algorithm suggested above, we derive here the fully pipelined architecture with table partitioning for FIR filters in highspeed and medium-speed. As described above, the structures in Ref. [8] have many latency as well as the number of adders. Therefore, here we make a modification on them to reduce the latency and the number of adders. First of all, the boundary adders of the two-dimensional (2-D) structure of Ref. [8] can be replaced by the pipelinedshift-adder tree. In the 2-D structure of Ref. [18], there are B number of shift adders in the boundary line (B is the word length of the input sample) and therefore the latency is B cycle periods.

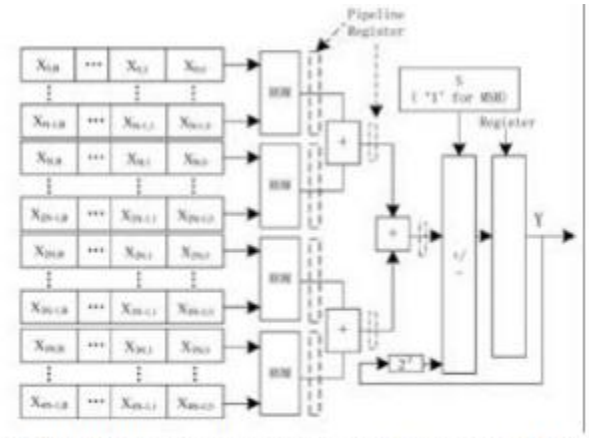

Fig. 2: FIR filters implementation with decomposed LUT's.

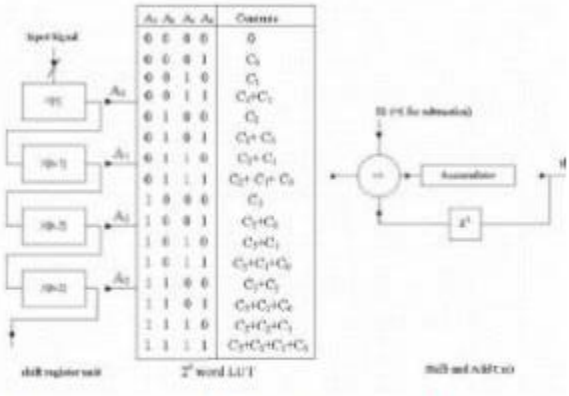

Fig. 3: Coeffcients update in Decomposed LUT.

The paper is structured as follows. Section 2 describes the problem statement. Section 3 depicts the Corner list representation. Section 4 reviews the mechanism of Hybrid PSOCS. Section 5 discusses experimental results. Finally, Section 6 concludes the paper.

Cuckoo Search (CS), originally introduced by Yang and Deb (2009) in 2009, is a new meta-heuristic search algorithm inspired by the behaviour of the bird cuckoo. CS uses Lévy flights rather than simple isotropic random walks. The advantage of CS is that it has fewer parameters to be fine-tuned when compared to genetic algorithm.

Let M be the set of modules represented by M= {m1, m2….mN}, where N is the number of modules. Each

module mi is represented by (Wi, Hi), where 1≤i≤N, Wi is width of the module mi and Hi is the height of the module mi. The aspect ratio of mi is defined as Hi / Wi. The area Ai of the module mi is given by Wi *Hi. There are three different kinds of rectangular modules namely soft modules, hard modules and pre-placed modules. The soft modules have variable aspect ratio within specified range and fixed area. In hard modules, both area and aspect ratio are fixed structure. The detailed description is given as follows:

Floorplanning is becoming more important for very large-scale integration (VLSI) physical design. Floorplanning is the process of planning the arrangement of modules in such a manner that area and interconnection wirelength should be minimized. According to Moore's Law, the number of transistors gets doubled for every eighteen months. This results in increasing the complexity of the circuits. The feature size of the IC is considerably scaled down, which results in an increase in search complexity. This makes the IC design more complex and corresponds to NP Hard Problem.

Two dummy modules mb and ml are located at the bottom and left boundaries respectively, corresponding to two lists: one for module and another for corners. Consider the module sequence (m4, m1, m2, m3), where module m4 is placed on the corner (mb, ml). The placement of the first module generates two corners (m4, ml) and (mb, m4) which is shown in Fig.3(a). Corner list array is updated containing two corners. Placing of the second module is done by randomly selecting any one of the corner from the list. Fig.3(b) shows that m1 is placed on the corner (m4, ml) and the selected corner is deleted from the array. Corner list is updated for every module placement. This process will be repeated for remaining modules placement as shown in Fig.3(c) and Fig.3(d). CL representation has more corners for selection than corner sequence representation. The property and theorems of CL are given below

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Proof: Let us consider that all the modules have different width and height. After placing the first module, there will be two corners in the corner list

their own nests. Once host bird recognises cuckoo egg, the host bird either destroys the cuckoo eggs out, or

host bird simply abandons its own nest and builds a new nest. Cuckoo bird choose a nest where host bird laid their eggs just before. Cuckoo egg hatches earlier as compared to that of host egg. After the cuckoo egg hatches, cuckoo chick evict host egg, which increases cuckoo's share of food provided by the host bird. Cuckoo search algorithm is based on the following three idealized rules.

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Some of the representations of the cuckoo search algorithm are each egg in a nest represents a solution and cuckoo can lay only one egg and to use the new and potentially better solutions to replace a bad solution in the nests. For simplicity purpose, each nest has only one egg. It uses a balanced combination of a local random walk and the global explorative random walk, controlled by a switching parameter pa.

5.1 Parameter settings for Algorithm: All the modules are considered as hard modules. The parameters of the PSO algorithm are set as follows: W=0.95, c1=2.1 and c2=2.1, number of particles will be in the range of 10 to 40 and it can be 10, which is large enough to get good results. The parameters of CS algorithm are set as follows: the probability or discovery rate of cuckoo egg pa =0.2 yields good result in terms of convergence rate. The number of host nest, which is also known as population size, n=15 is efficient for most optimization problems.

Conclusion

In this paper, we have proposed hybrid of cuckoo search and PSO algorithm in order to solve nonslicingfloorplan in efficient manner. Corner list representation is a new floorplan representation and it is used to represent non-slicing floorplan. The experimental results for MCNC benchmark circuits demonstrated that the proposed algorithm can able to achieve the optimal result for hard modules placement.The future work will focus on the parameter related to some constraints.

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